

# Compal Confidential

## KAWF0/KAWH0 M/B Schematics Document

### Intel Penryn Processor with Cantiga + DDRII + ICH9M

2009-01-21

REV:1.0

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Issued Date	2009/01/21	Deciphered Date	2010/01/21	Title	SCHEMATIC, M/B A4851
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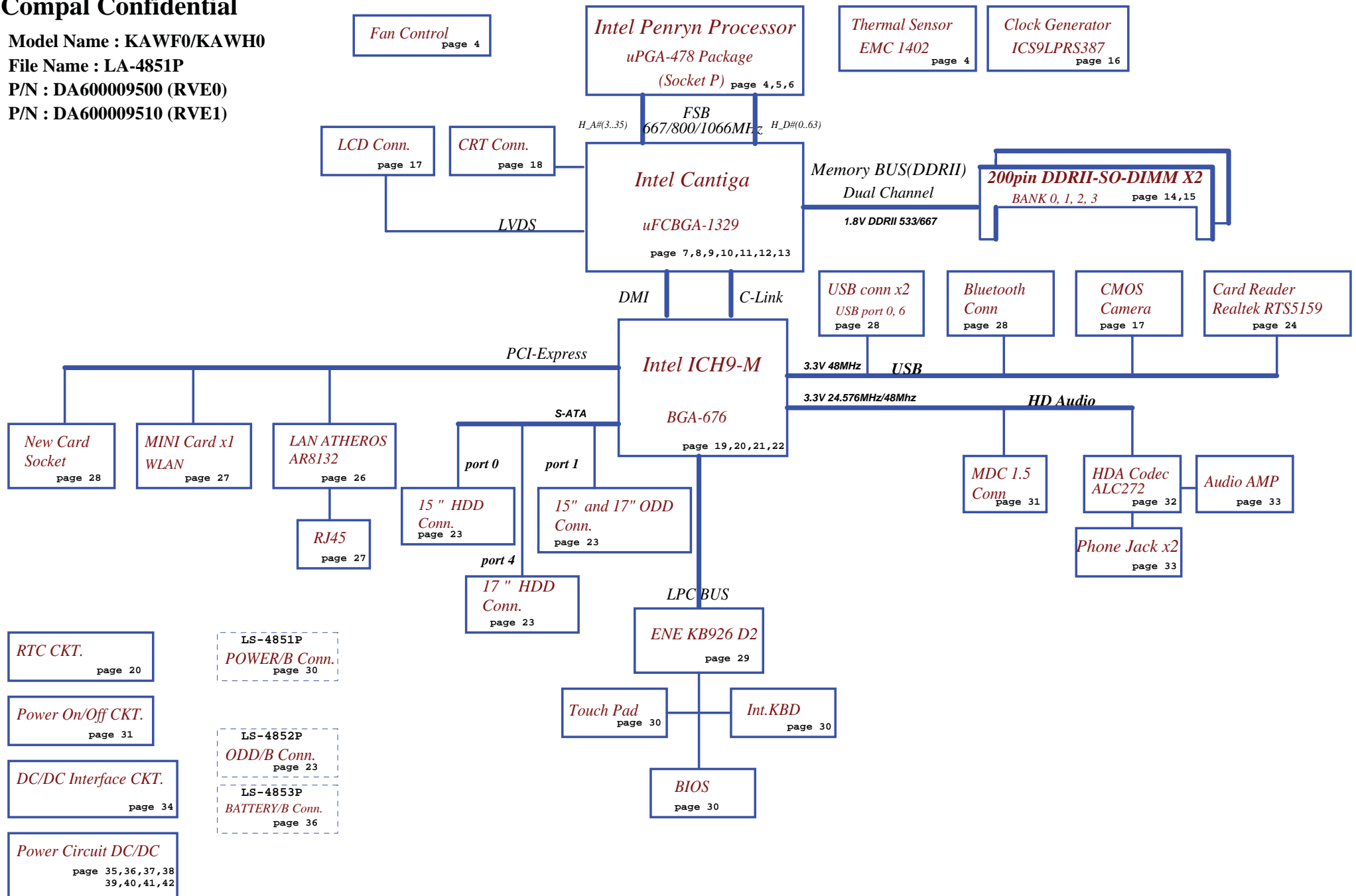
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Model Name : KAWF0/KAWH0

File Name : LA-4851P

P/N : DA600009500 (RVE0)

P/N : DA600009510 (RVE1)



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### Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

### External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
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### EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

### EC SM Bus2 address

### ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS367, SLG8SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

### Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

### BTO Option Table

BTO Item	BOM Structure
GM45	GM@
GL40	GL@
15"	15@
17"	17@
8114	8114@
8132	8132@

### PCIE table

PCIE port1	Express Card(Reserved)
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

### SATA table

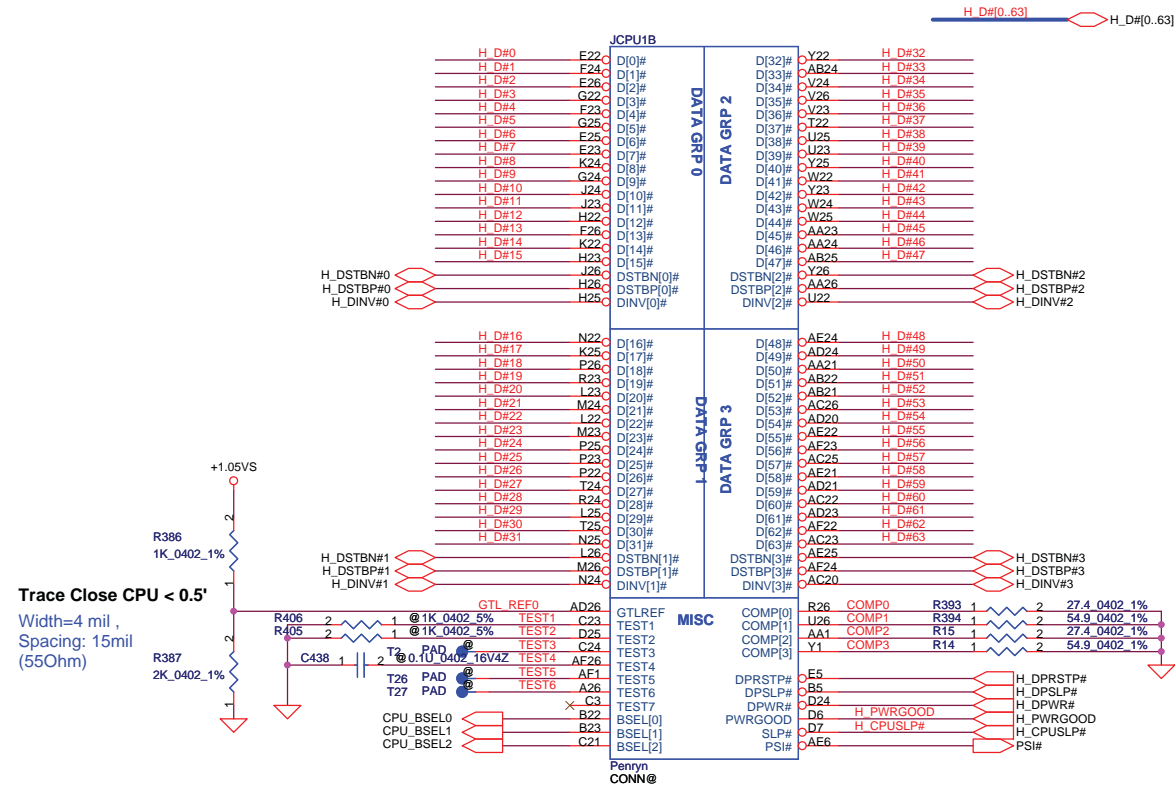
SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	for 17" 2nd HDD
SATA port5	

### USB table

EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	
	UHCI2	Port2	
		Port3	CMOS Camera
EHCI2	UHCI3	Port4	Card Reader
		Port5	New Card(Reserved)
	UHCI4	Port6	MB USB Conn.
		Port7	
	UHCI5	Port8	Blue Tooth
		Port9	
	UHCI6	Port10	Wireless Card
		Port11	

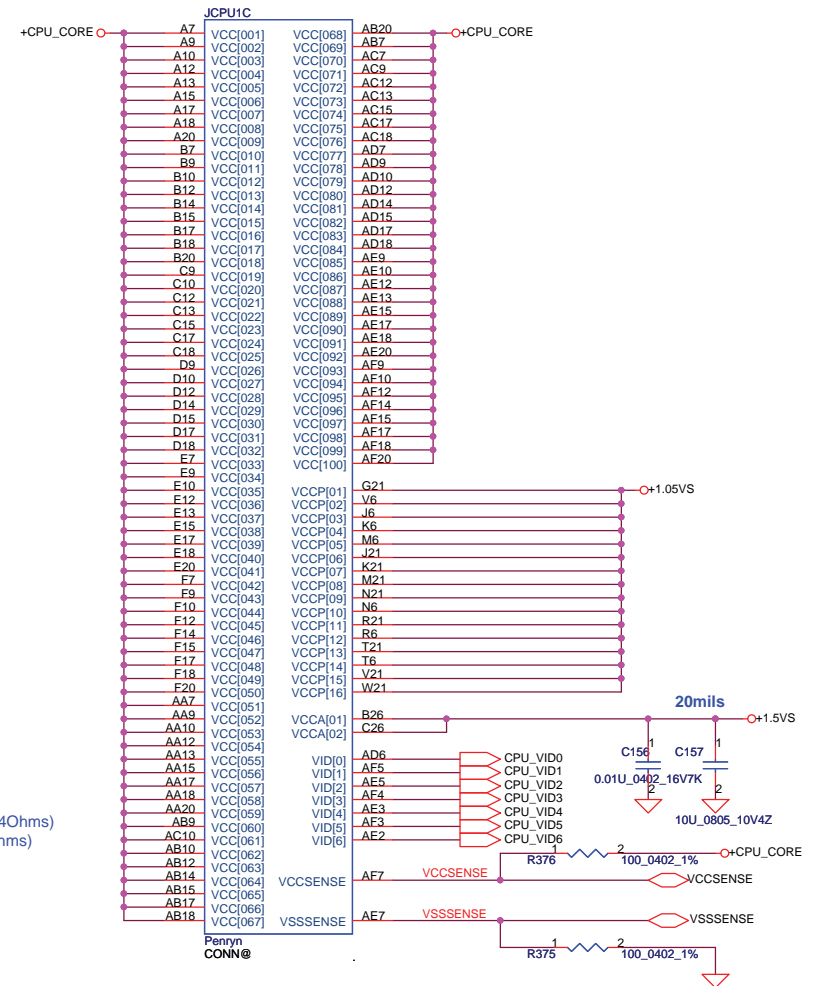


Trace Close CPU < 0.5'  
Width=4 mil,  
Spacing: 15mil  
(55Ohm)

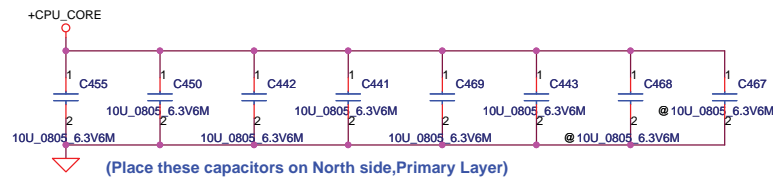
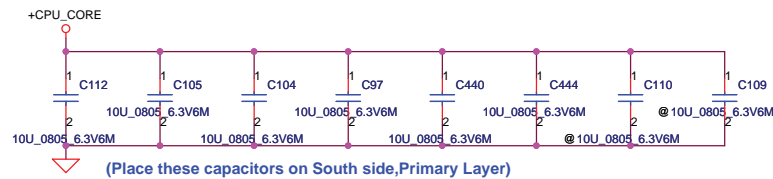
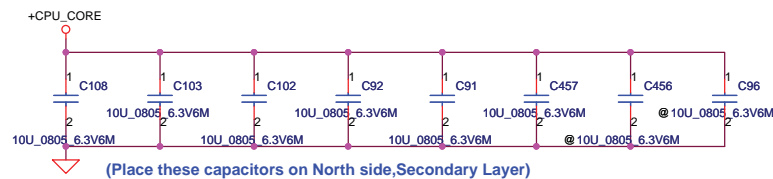
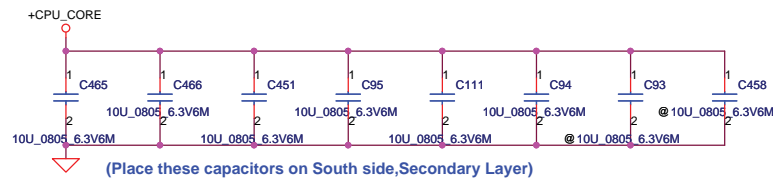
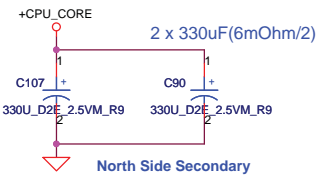
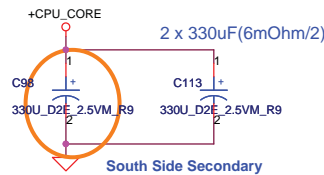
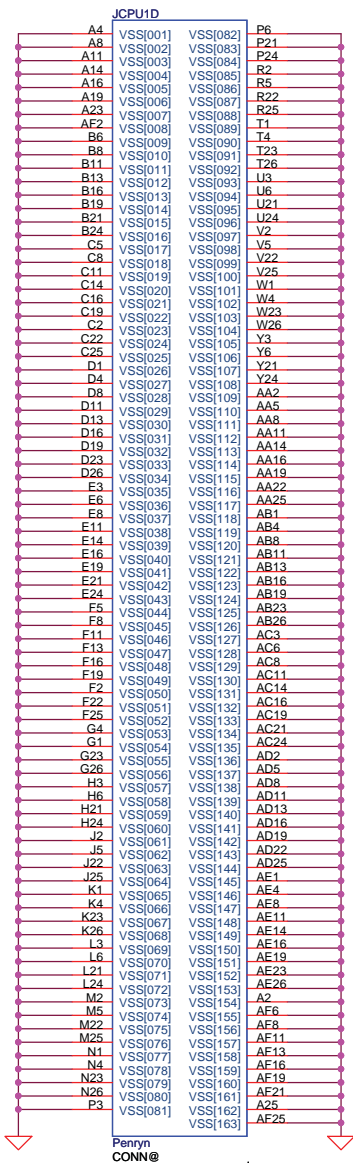


TRACE CLOSELY CPU < 0.5'

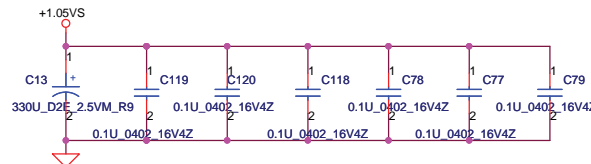
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)  
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)



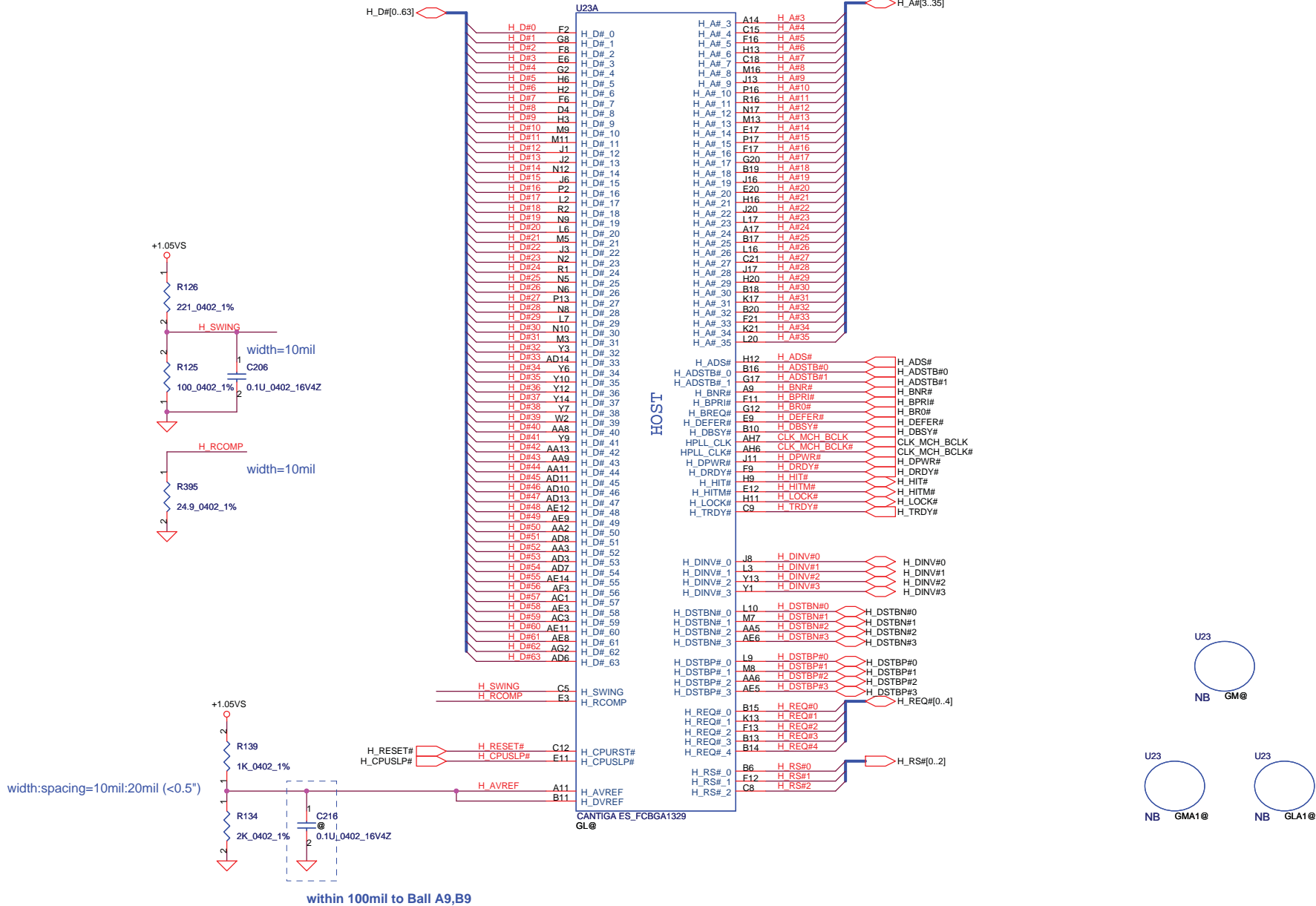
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+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



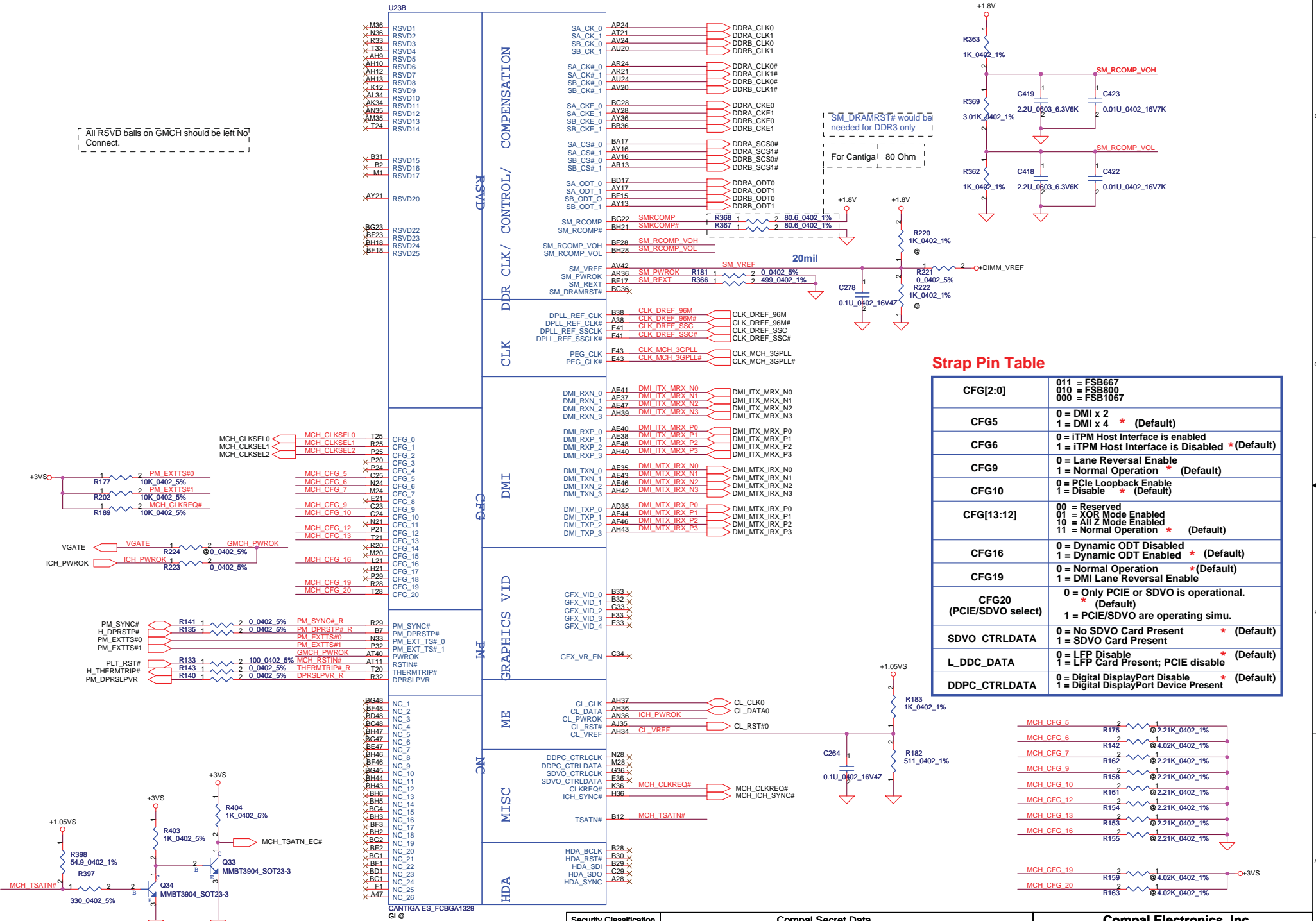
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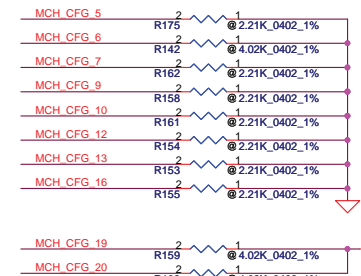


All RSVD balls on GMCH should be left No Connect.



Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable 1 = LFP Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present * (Default)





DDRA\_SDQ[0..63] <== DDRA\_SDQ[0..63]  
DDRA\_SDM[0..7] <== DDRA\_SDM[0..7]  
DDRA\_SMA[0..14] <== DDRA\_SMA[0..14]

DDRB\_SDQ[0..63] <== DDRB\_SDQ[0..63]  
DDRB\_SDM[0..7] <== DDRB\_SDM[0..7]  
DDRB\_SMA[0..14] <== DDRB\_SMA[0..14]

U23D			
DDRA_SDQ0	AJ38	SA_DQ_0	
DDRA_SDQ1	AJ41	SA_DQ_1	
DDRA_SDQ2	AN38	SA_DQ_2	
DDRA_SDQ3	AM38	SA_DQ_3	
DDRA_SDQ4	AJ36	SA_DQ_4	
DDRA_SDQ5	AJ40	SA_DQ_5	
DDRA_SDQ6	AM44	SA_DQ_6	
DDRA_SDQ7	AM42	SA_DQ_7	
DDRA_SDQ8	AN43	SA_DQ_8	
DDRA_SDQ9	AN44	SA_DQ_9	
DDRA_SDQ10	AJ40	SA_DQ_10	
DDRA_SDQ11	AT38	SA_DQ_11	
DDRA_SDQ12	AN41	SA_DQ_12	
DDRA_SDQ13	AN39	SA_DQ_13	
DDRA_SDQ14	AJ44	SA_DQ_14	
DDRA_SDQ15	AJ42	SA_DQ_15	
DDRA_SDQ16	AV39	SA_DQ_16	
DDRA_SDQ17	AY44	SA_DQ_17	
DDRA_SDQ18	BA40	SA_DQ_18	
DDRA_SDQ19	BD43	SA_DQ_19	
DDRA_SDQ20	AY41	SA_DQ_20	
DDRA_SDQ21	AY43	SA_DQ_21	
DDRA_SDQ22	BB41	SA_DQ_22	
DDRA_SDQ23	BC40	SA_DQ_23	
DDRA_SDQ24	AY37	SA_DQ_24	
DDRA_SDQ25	BD38	SA_DQ_25	
DDRA_SDQ26	AV37	SA_DQ_26	
DDRA_SDQ27	AT36	SA_DQ_27	
DDRA_SDQ28	AY38	SA_DQ_28	
DDRA_SDQ29	BB38	SA_DQ_29	
DDRA_SDQ30	AV36	SA_DQ_30	
DDRA_SDQ31	AW36	SA_DQ_31	
DDRA_SDQ32	BD13	SA_DQ_32	
DDRA_SDQ33	AJ11	SA_DQ_33	
DDRA_SDQ34	BC11	SA_DQ_34	
DDRA_SDQ35	BA12	SA_DQ_35	
DDRA_SDQ36	AJ13	SA_DQ_36	
DDRA_SDQ37	AV13	SA_DQ_37	
DDRA_SDQ38	BD12	SA_DQ_38	
DDRA_SDQ39	BC12	SA_DQ_39	
DDRA_SDQ40	BB9	SA_DQ_40	
DDRA_SDQ41	BA9	SA_DQ_41	
DDRA_SDQ42	AJ10	SA_DQ_42	
DDRA_SDQ43	AV9	SA_DQ_43	
DDRA_SDQ44	BA11	SA_DQ_44	
DDRA_SDQ45	BD9	SA_DQ_45	
DDRA_SDQ46	AY8	SA_DQ_46	
DDRA_SDQ47	BA6	SA_DQ_47	
DDRA_SDQ48	AV5	SA_DQ_48	
DDRA_SDQ49	AV7	SA_DQ_49	
DDRA_SDQ50	AT9	SA_DQ_50	
DDRA_SDQ51	AN8	SA_DQ_51	
DDRA_SDQ52	AJ5	SA_DQ_52	
DDRA_SDQ53	AJ6	SA_DQ_53	
DDRA_SDQ54	AT5	SA_DQ_54	
DDRA_SDQ55	AN10	SA_DQ_55	
DDRA_SDQ56	AM11	SA_DQ_56	
DDRA_SDQ57	AM5	SA_DQ_57	
DDRA_SDQ58	AJ9	SA_DQ_58	
DDRA_SDQ59	AJ8	SA_DQ_59	
DDRA_SDQ60	AN12	SA_DQ_60	
DDRA_SDQ61	AM13	SA_DQ_61	
DDRA_SDQ62	AJ11	SA_DQ_62	
DDRA_SDQ63	AJ12	SA_DQ_63	

DDR SYSTEM MEMORY A

SA_BS_0	BD21	DDRA_SBS0#
SA_BS_1	BG18	DDRA_SBS1#
SA_BS_2	AT25	DDRA_SBS2#
SA_RAS#	BB20	DDRA_SRAS#
SA_CAS#	BD20	DDRA_SCAS#
SA_WE#	AY20	DDRA_SWE#
SA_DM_0	AM37	DDRA_SDM0
SA_DM_1	AT41	DDRA_SDM1
SA_DM_2	AY41	DDRA_SDM2
SA_DM_3	AJ39	DDRA_SDM3
SA_DM_4	BB12	DDRA_SDM4
SA_DM_5	AY6	DDRA_SDM5
SA_DM_6	AT7	DDRA_SDM6
SA_DM_7	AJ5	DDRA_SDM7
SA_DQS_0	AJ44	DDRA_SDQS0
SA_DQS_1	AT44	DDRA_SDQS1
SA_DQS_2	BA43	DDRA_SDQS2
SA_DQS_3	BC37	DDRA_SDQS3
SA_DQS_4	AW12	DDRA_SDQS4
SA_DQS_5	BC8	DDRA_SDQS5
SA_DQS_6	AJ8	DDRA_SDQS6
SA_DQS_7	AM7	DDRA_SDQS7
SA_DQS_0	AJ43	DDRA_SDQS0#
SA_DQS_1	AT43	DDRA_SDQS1#
SA_DQS_2	BA44	DDRA_SDQS2#
SA_DQS_3	BD37	DDRA_SDQS3#
SA_DQS_4	AY12	DDRA_SDQS4#
SA_DQS_5	BD8	DDRA_SDQS5#
SA_DQS_6	AJ9	DDRA_SDQS6#
SA_DQS_7	AM8	DDRA_SDQS7#
SA_MA_0	BA21	DDRA_SMA0
SA_MA_1	BC24	DDRA_SMA1
SA_MA_2	BG24	DDRA_SMA2
SA_MA_3	BH24	DDRA_SMA3
SA_MA_4	BG25	DDRA_SMA4
SA_MA_5	BA24	DDRA_SMA5
SA_MA_6	BD24	DDRA_SMA6
SA_MA_7	BC27	DDRA_SMA7
SA_MA_8	BF25	DDRA_SMA8
SA_MA_9	AW24	DDRA_SMA9
SA_MA_10	BC21	DDRA_SMA10
SA_MA_11	BG26	DDRA_SMA11
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SA_MA_13	BH17	DDRA_SMA13
SA_MA_14	AY25	DDRA_SMA14

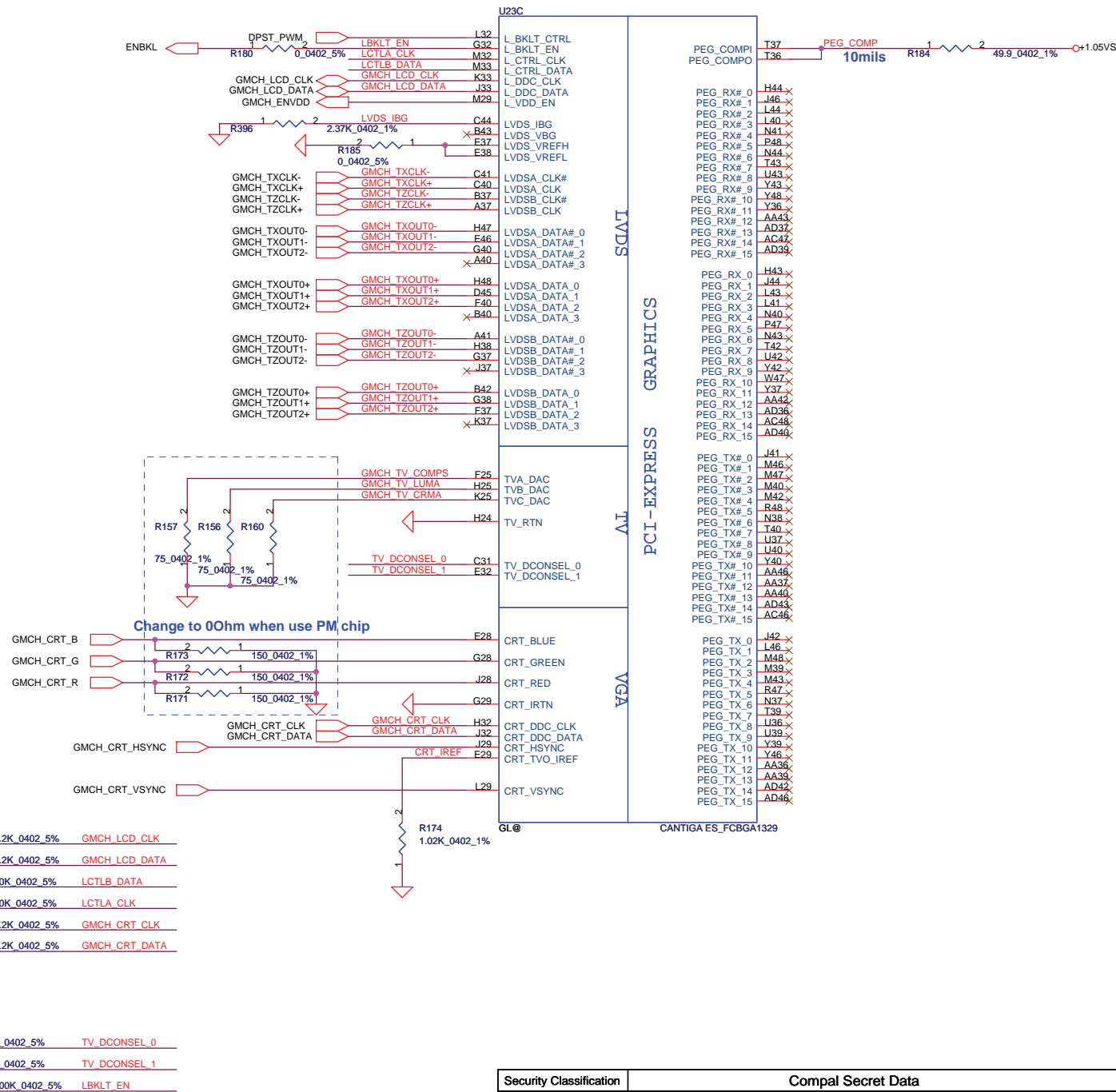
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U23E			
DDRB_SDQ0	AK47	SB_DQ_0	
DDRB_SDQ1	AH46	SB_DQ_1	
DDRB_SDQ2	AP47	SB_DQ_2	
DDRB_SDQ3	AP46	SB_DQ_3	
DDRB_SDQ4	AJ46	SB_DQ_4	
DDRB_SDQ5	AJ48	SB_DQ_5	
DDRB_SDQ6	AM48	SB_DQ_6	
DDRB_SDQ7	AP48	SB_DQ_7	
DDRB_SDQ8	AJ47	SB_DQ_8	
DDRB_SDQ9	AJ46	SB_DQ_9	
DDRB_SDQ10	BA48	SB_DQ_10	
DDRB_SDQ11	AY48	SB_DQ_11	
DDRB_SDQ12	AT47	SB_DQ_12	
DDRB_SDQ13	AR47	SB_DQ_13	
DDRB_SDQ14	BA47	SB_DQ_14	
DDRB_SDQ15	BC47	SB_DQ_15	
DDRB_SDQ16	BC46	SB_DQ_16	
DDRB_SDQ17	BC44	SB_DQ_17	
DDRB_SDQ18	BG43	SB_DQ_18	
DDRB_SDQ19	BE43	SB_DQ_19	
DDRB_SDQ20	BE45	SB_DQ_20	
DDRB_SDQ21	BC41	SB_DQ_21	
DDRB_SDQ22	BE40	SB_DQ_22	
DDRB_SDQ23	BC41	SB_DQ_23	
DDRB_SDQ24	BC38	SB_DQ_24	
DDRB_SDQ25	BC38	SB_DQ_25	
DDRB_SDQ26	BH35	SB_DQ_26	
DDRB_SDQ27	BG35	SB_DQ_27	
DDRB_SDQ28	BH40	SB_DQ_28	
DDRB_SDQ29	BC39	SB_DQ_29	
DDRB_SDQ30	BG34	SB_DQ_30	
DDRB_SDQ31	BH34	SB_DQ_31	
DDRB_SDQ32	BH14	SB_DQ_32	
DDRB_SDQ33	BG12	SB_DQ_33	
DDRB_SDQ34	BH11	SB_DQ_34	
DDRB_SDQ35	BG8	SB_DQ_35	
DDRB_SDQ36	BH12	SB_DQ_36	
DDRB_SDQ37	BF11	SB_DQ_37	
DDRB_SDQ38	BF8	SB_DQ_38	
DDRB_SDQ39	BG7	SB_DQ_39	
DDRB_SDQ40	BC5	SB_DQ_40	
DDRB_SDQ41	BC6	SB_DQ_41	
DDRB_SDQ42	AY3	SB_DQ_42	
DDRB_SDQ43	AY1	SB_DQ_43	
DDRB_SDQ44	BF5	SB_DQ_44	
DDRB_SDQ45	BF5	SB_DQ_45	
DDRB_SDQ46	BA1	SB_DQ_46	
DDRB_SDQ47	BD3	SB_DQ_47	
DDRB_SDQ48	AV2	SB_DQ_48	
DDRB_SDQ49	AJ3	SB_DQ_49	
DDRB_SDQ50	AR3	SB_DQ_50	
DDRB_SDQ51	AN2	SB_DQ_51	
DDRB_SDQ52	AY2	SB_DQ_52	
DDRB_SDQ53	AV1	SB_DQ_53	
DDRB_SDQ54	AP3	SB_DQ_54	
DDRB_SDQ55	AR1	SB_DQ_55	
DDRB_SDQ56	AL1	SB_DQ_56	
DDRB_SDQ57	AL2	SB_DQ_57	
DDRB_SDQ58	AJ1	SB_DQ_58	
DDRB_SDQ59	AH1	SB_DQ_59	
DDRB_SDQ60	AM2	SB_DQ_60	
DDRB_SDQ61	AM3	SB_DQ_61	
DDRB_SDQ62	AH3	SB_DQ_62	
DDRB_SDQ63	AJ3	SB_DQ_63	
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SB_BS_1	BB17		DDRB_SBS1#
SB_BS_2	BB33		DDRB_SBS2#
SB_RAS#	AJ17		DDRB_SRAS#
SB_CAS#	BG16		DDRB_SCAS#
SB_WE#	BF14		DDRB_SWE#
SB_DM_0	AM47	DDRB_SDM0	
SB_DM_1	AY47	DDRB_SDM1	
SB_DM_2	BD40	DDRB_SDM2	
SB_DM_3	BF35	DDRB_SDM3	
SB_DM_4	BG11	DDRB_SDM4	
SB_DM_5	BA3	DDRB_SDM5	
SB_DM_6	AP1	DDRB_SDM6	
SB_DM_7	AK2	DDRB_SDM7	
SB_DQS_0	AL47	DDRB_SDQS0	
SB_DQS_1	AV48	DDRB_SDQS1	DDRB_SDQS0
SB_DQS_2	BG41	DDRB_SDQS2	DDRB_SDQS2
SB_DQS_3	BG37	DDRB_SDQS3	DDRB_SDQS3
SB_DQS_4	BH9	DDRB_SDQS4	DDRB_SDQS4
SB_DQS_5	BB2	DDRB_SDQS5	DDRB_SDQS5
SB_DQS_6	AJ1	DDRB_SDQS6	DDRB_SDQS6
SB_DQS_7	AN6	DDRB_SDQS7	DDRB_SDQS7
SB_DQS_0	AL46	DDRB_SDQS0#	DDRB_SDQS0#
SB_DQS_1	AV47	DDRB_SDQS1#	DDRB_SDQS1#
SB_DQS_2	BH41	DDRB_SDQS2#	DDRB_SDQS2#
SB_DQS_3	BH37	DDRB_SDQS3#	DDRB_SDQS3#
SB_DQS_4	BG9	DDRB_SDQS4#	DDRB_SDQS4#
SB_DQS_5	BC2	DDRB_SDQS5#	DDRB_SDQS5#
SB_DQS_6	AT2	DDRB_SDQS6#	DDRB_SDQS6#
SB_DQS_7	AN5	DDRB_SDQS7#	DDRB_SDQS7#
SB_MA_0	AV17	DDRB_SMA0	
SB_MA_1	BA25	DDRB_SMA1	
SB_MA_2	BC25	DDRB_SMA2	
SB_MA_3	AU25	DDRB_SMA3	
SB_MA_4	AW25	DDRB_SMA4	
SB_MA_5	BB28	DDRB_SMA5	
SB_MA_6	AU28	DDRB_SMA6	
SB_MA_7	AW28	DDRB_SMA7	
SB_MA_8	AT33	DDRB_SMA8	
SB_MA_9	BD33	DDRB_SMA9	
SB_MA_10	BB16	DDRB_SMA10	
SB_MA_11	AW33	DDRB_SMA11	
SB_MA_12	AY33	DDRB_SMA12	
SB_MA_13	BH15	DDRB_SMA13	
SB_MA_14	AJ33	DDRB_SMA14	

DDR SYSTEM MEMORY B

GL@ CANTIGA ES\_FCBGA1329

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								Custom	401636			D	
								Date: Monday, February 09, 2009			Sheet 10 of 45		

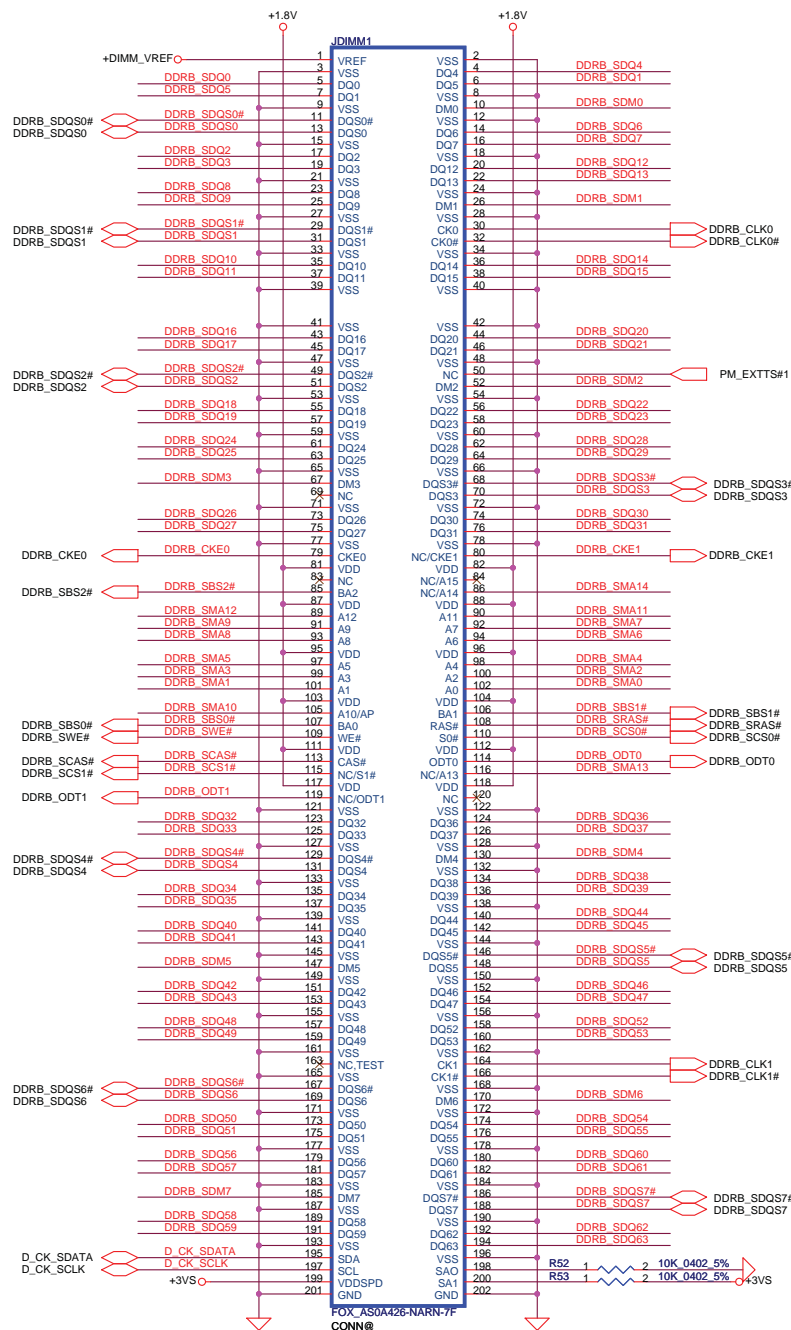




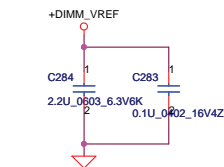




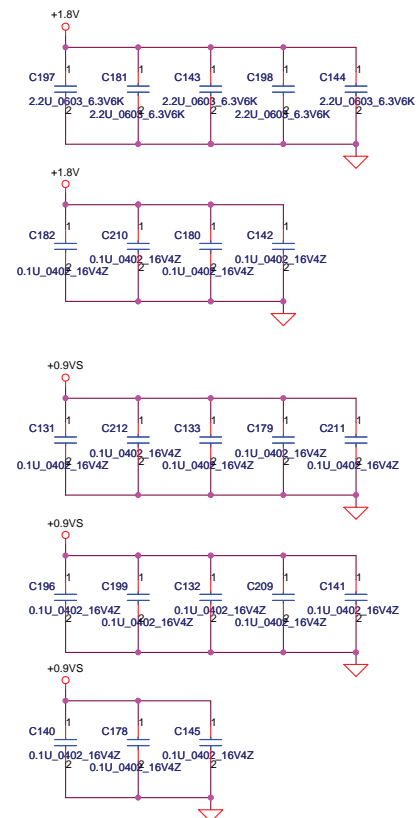
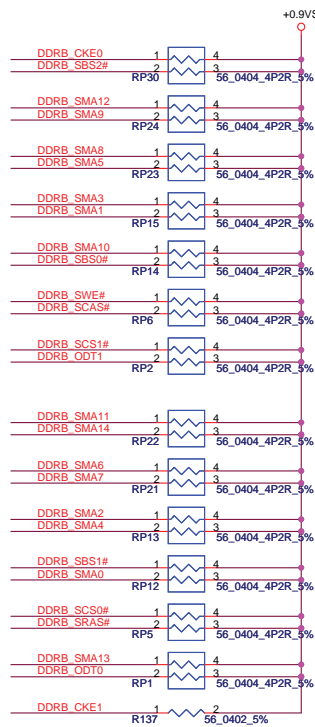
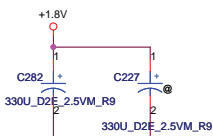




**DIMM1 REV H:9.2mm (BOT)**



DDR\_B\_SMA[0..14] → DDRB\_SMA[0..14]  
 DDRB\_SQ[0..63] → DDRB\_SQ[0..63]  
 DDRB\_SDM[0..7] → DDRB\_SDM[0..7]



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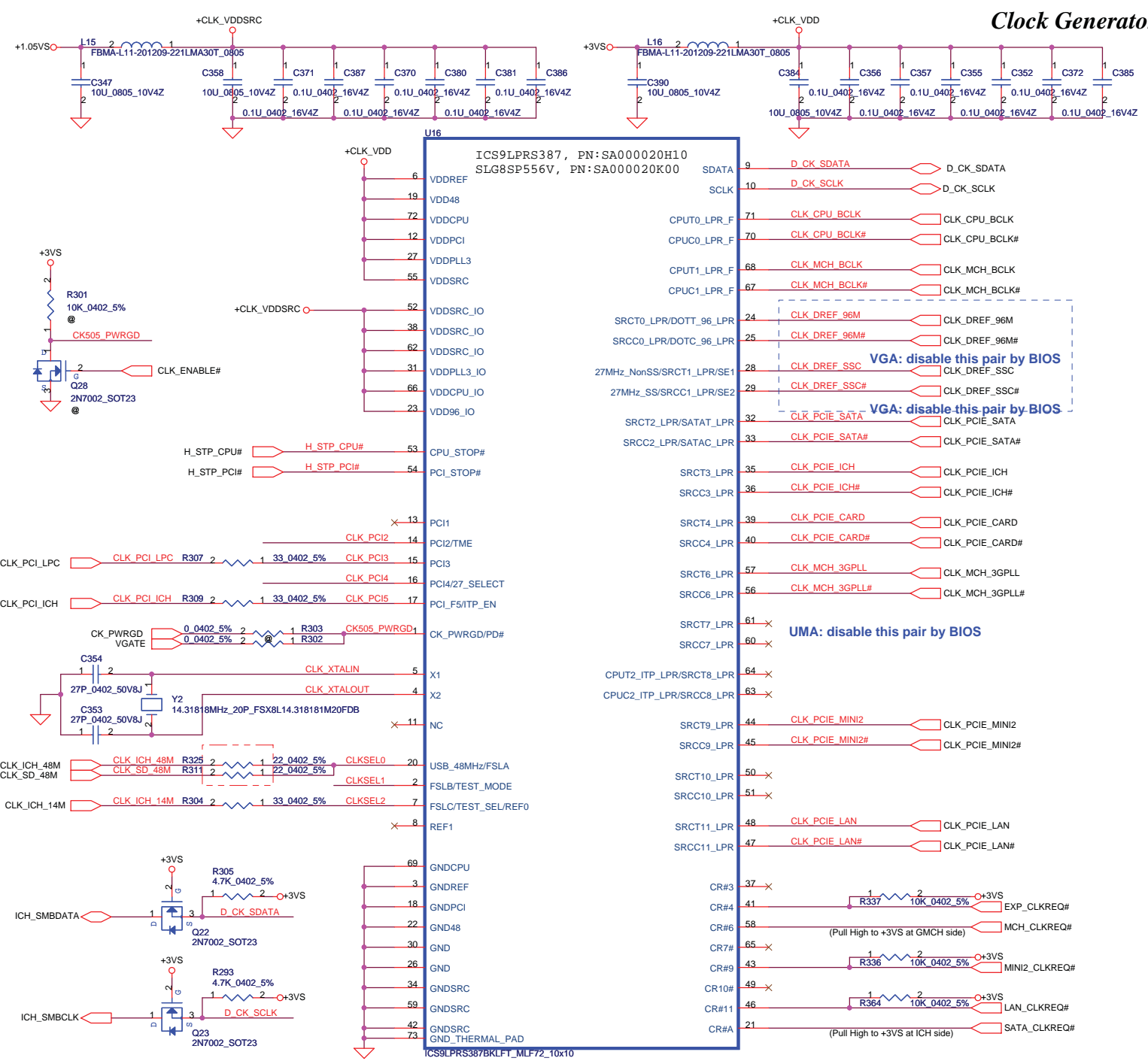
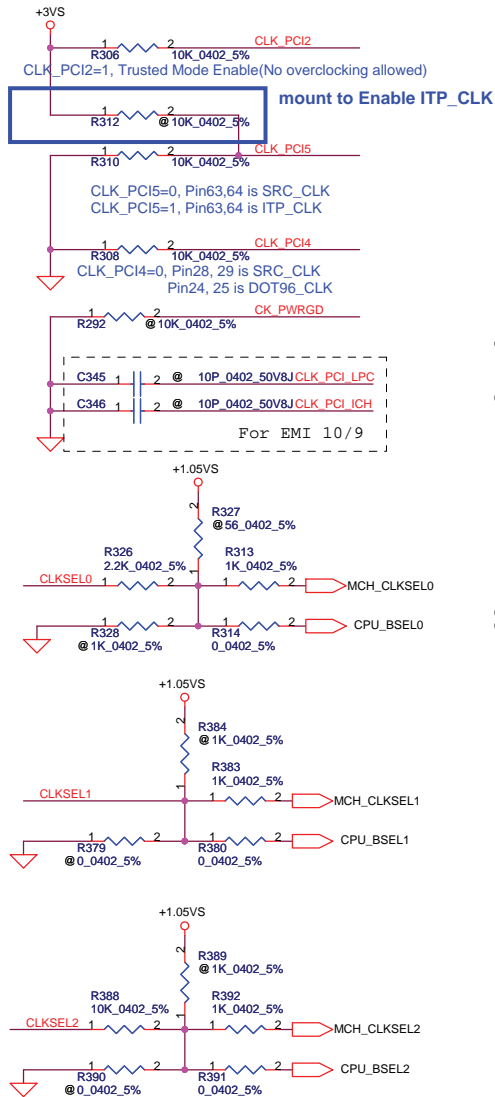


FSLC	FSLB	FSLA	CPU	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

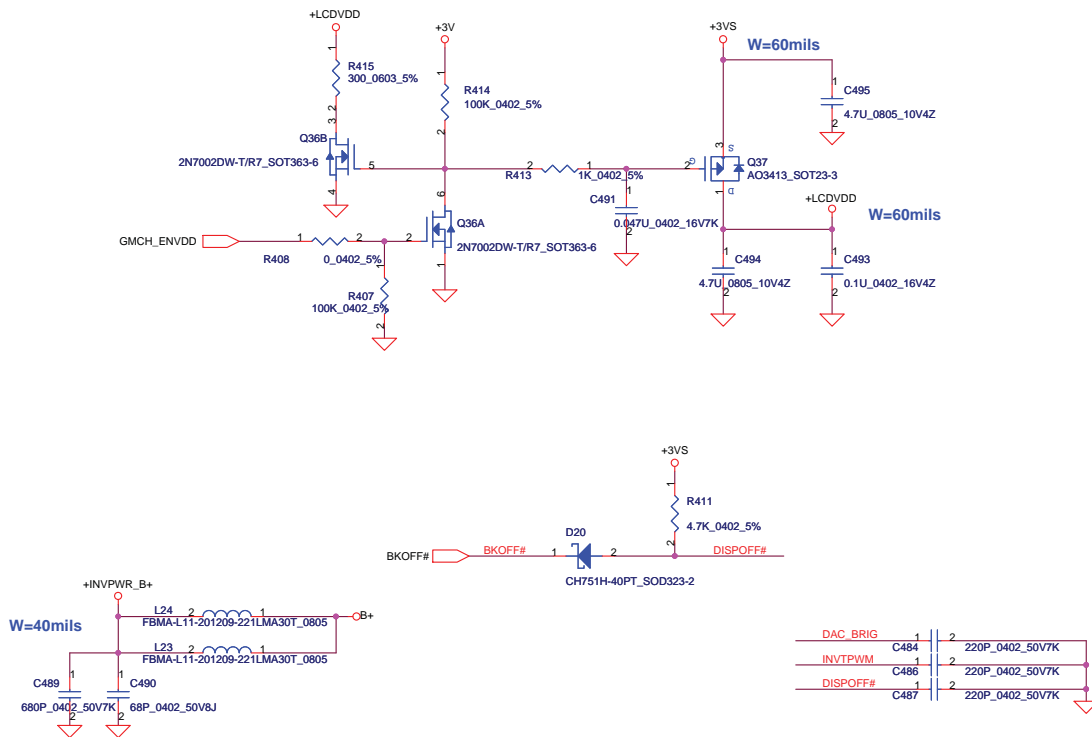
SRCT7(VGA\_CLK): Discrete VGA[Enable] UMA[Disable]



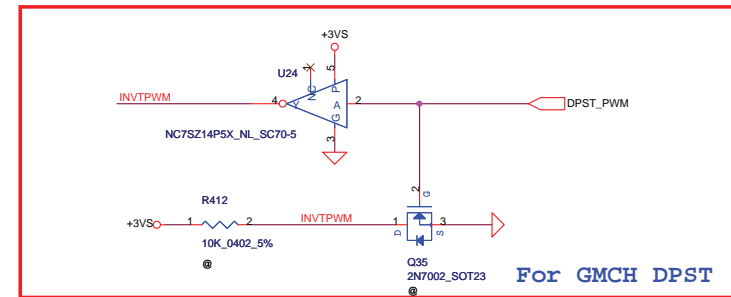
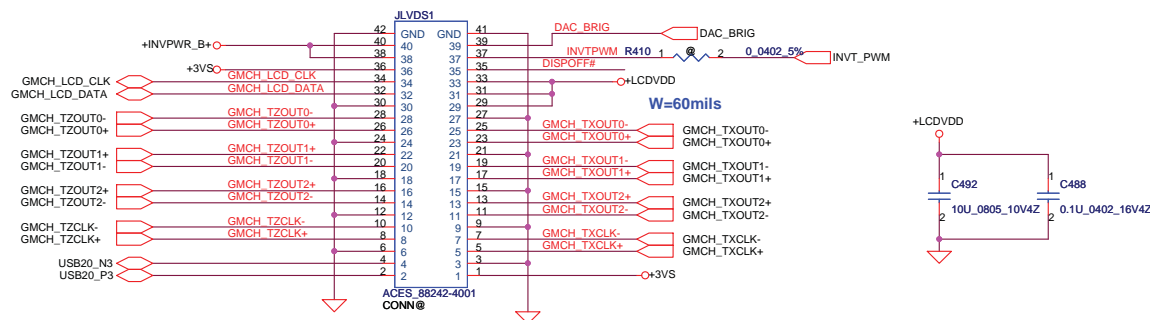
## Clock Generator

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## LCD POWER CIRCUIT



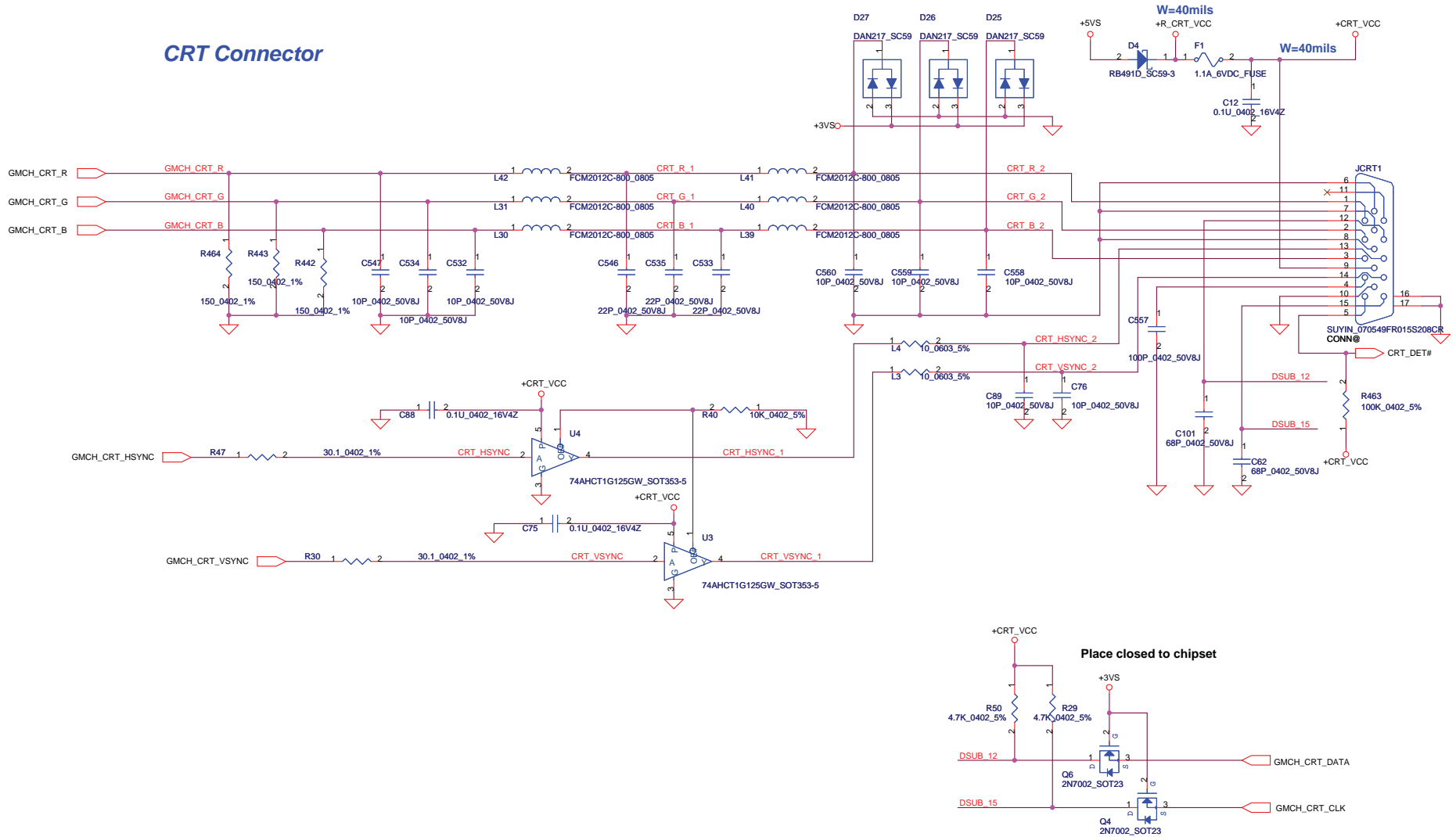
LCD/PANEL BD. Conn.



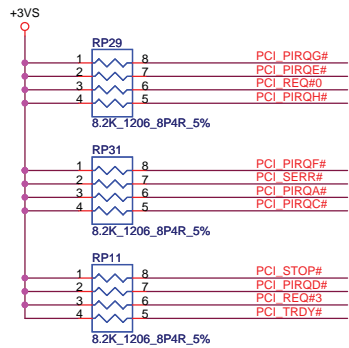
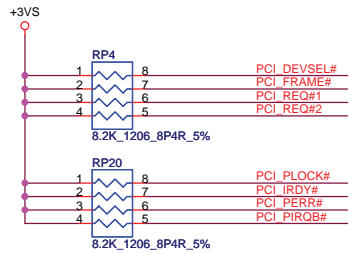
For GMCH DPST

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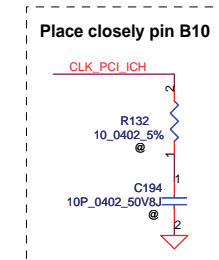
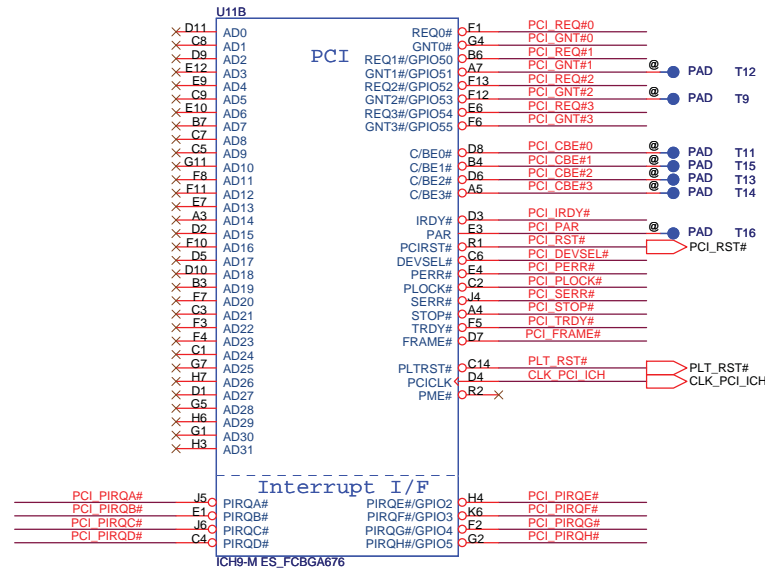
# CRT Connector



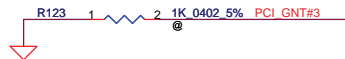
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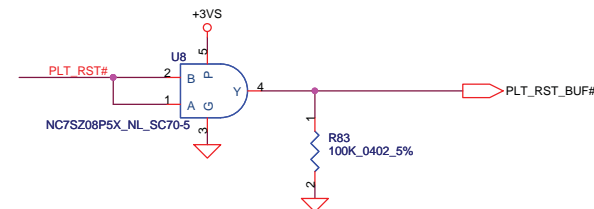
**DMI for ESI-compatible operation**  
**PCI\_GNT#1** Low= DMI for ESI-compatible operation  
 High= Default\* (Internal pull-up)



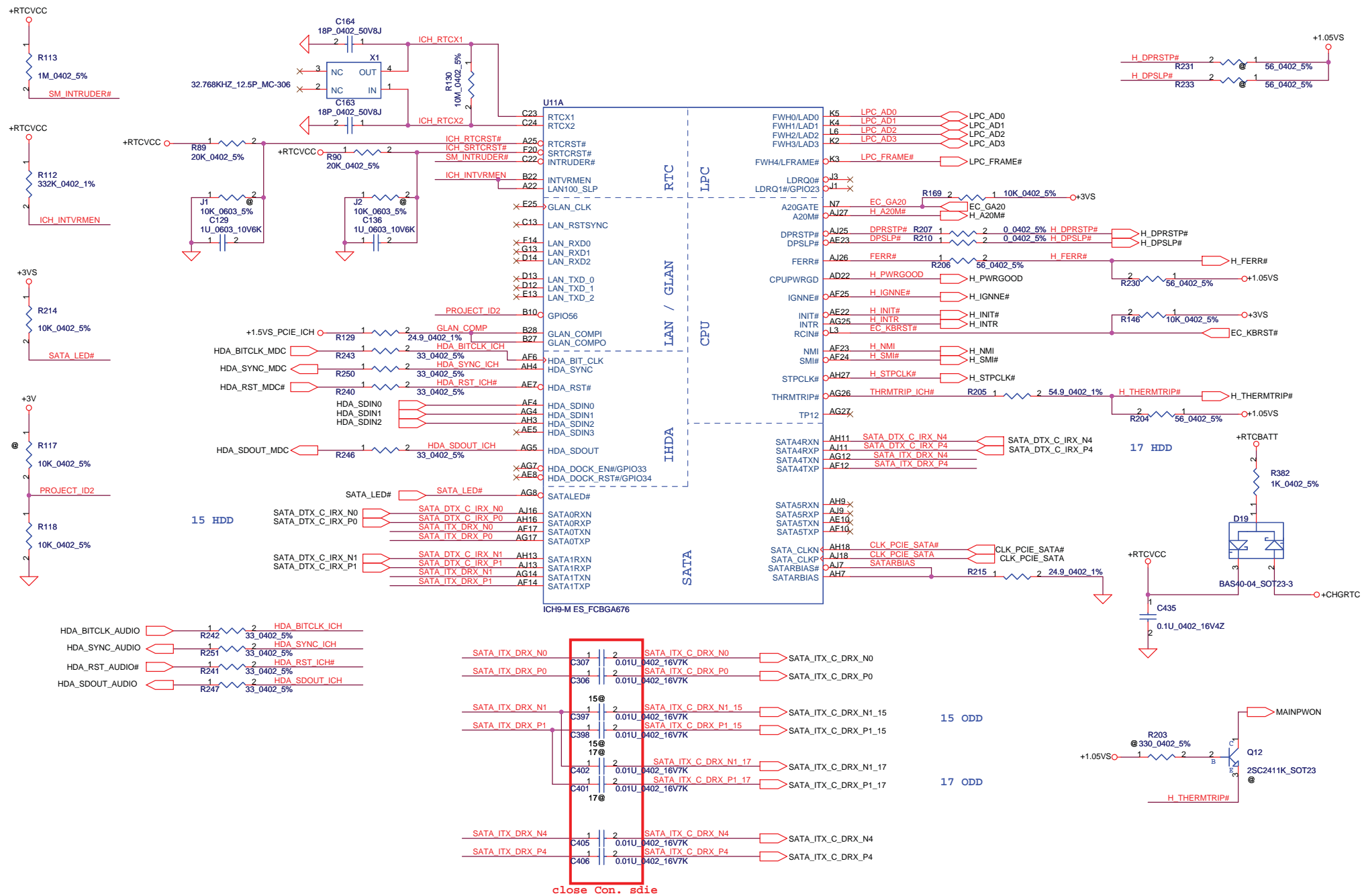
**A16 Swap Override Strap**  
**PCI\_GNT#3** Low= A16 swap override Enable  
 High= Default\*



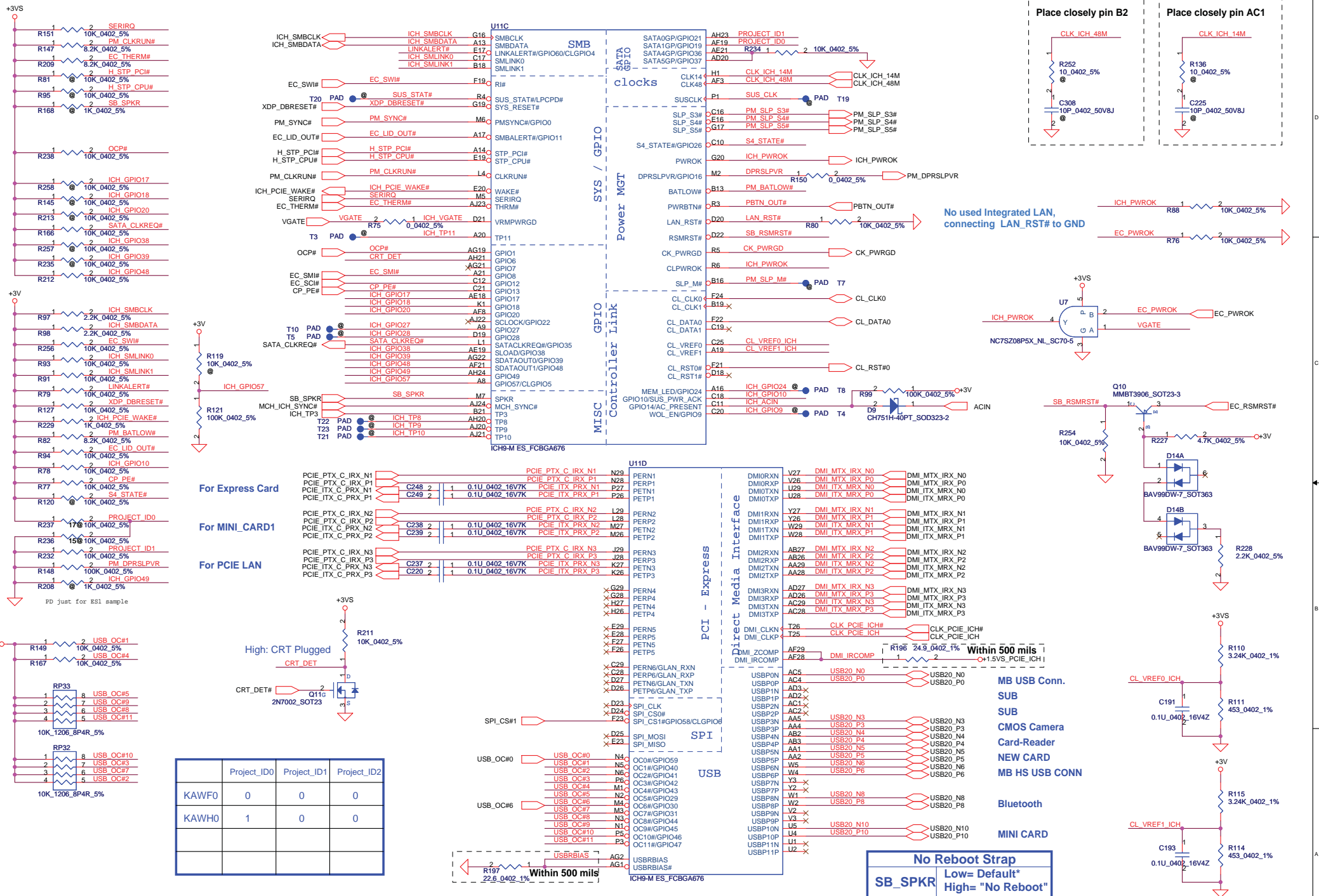
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



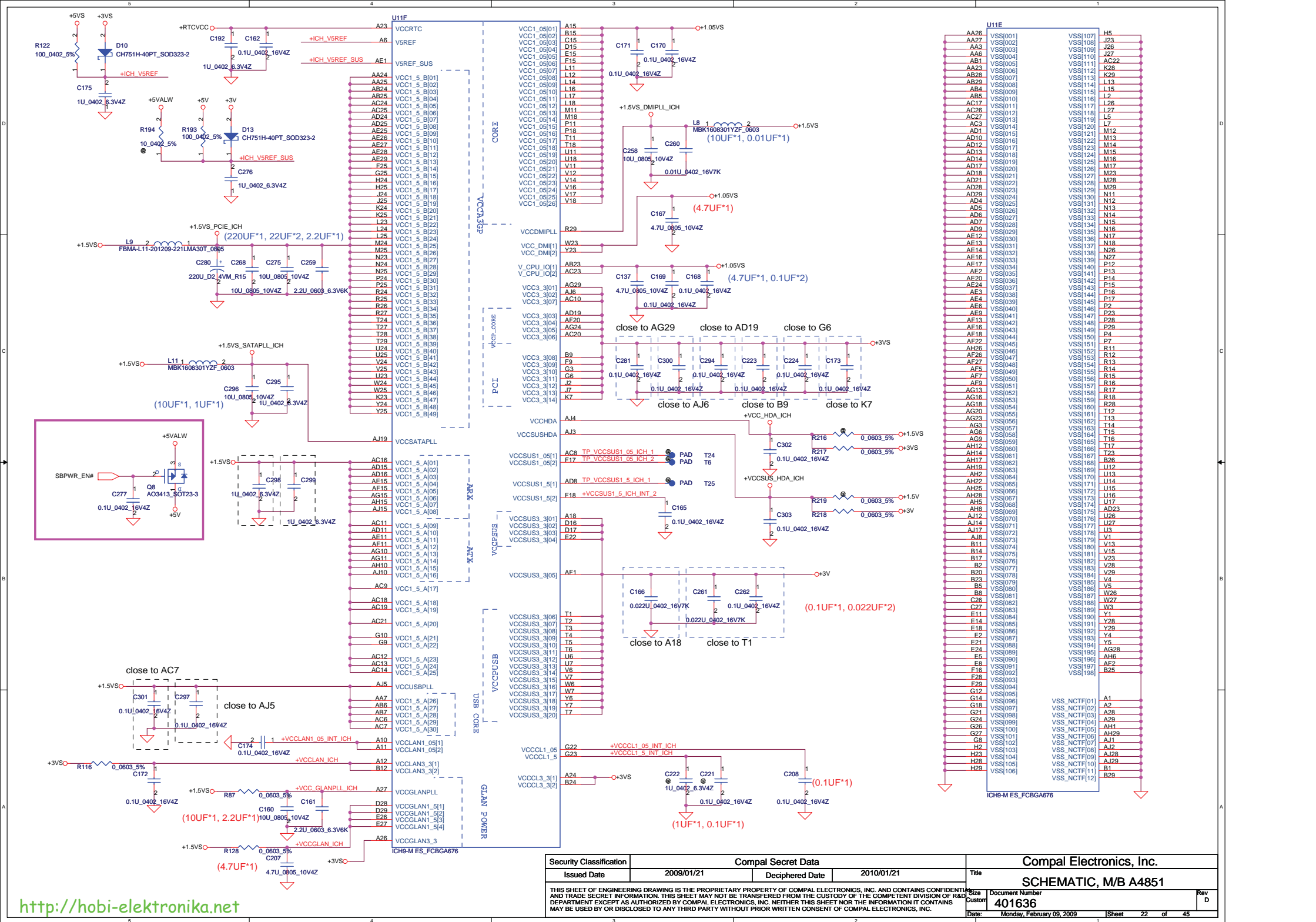
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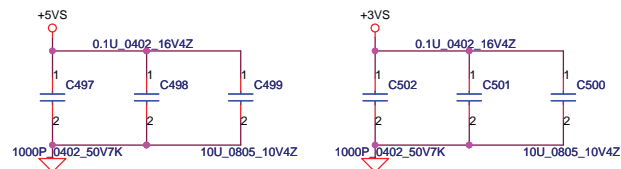
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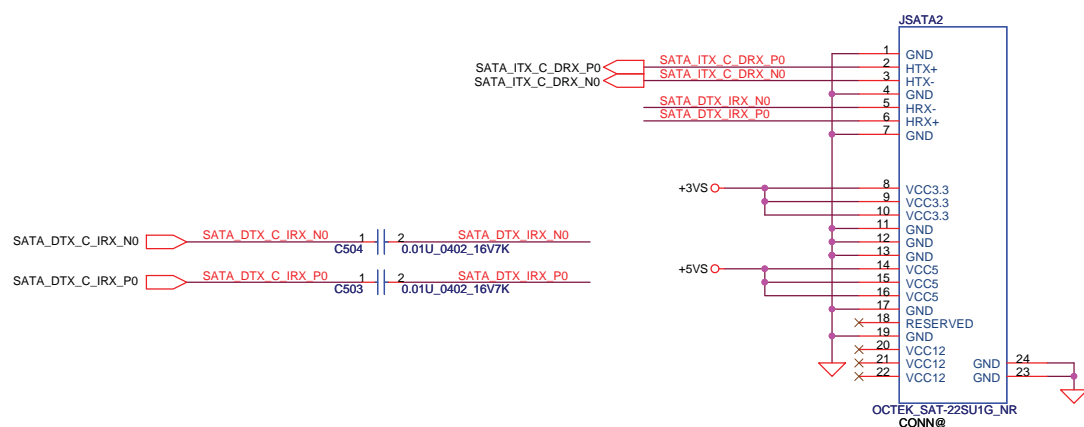




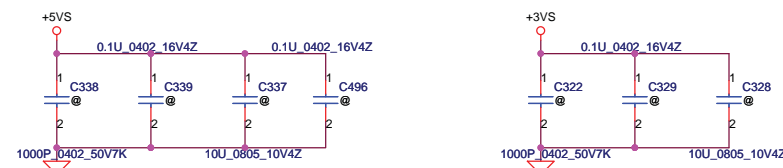
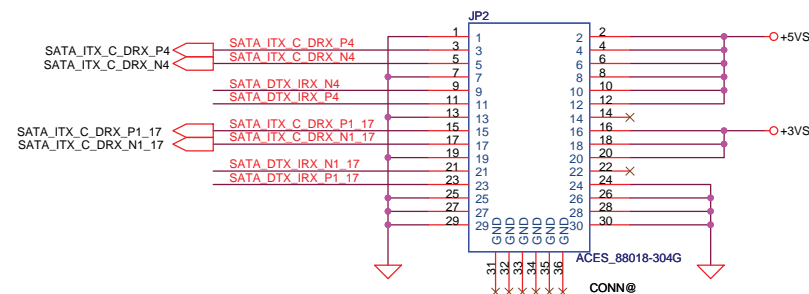
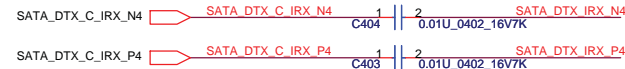
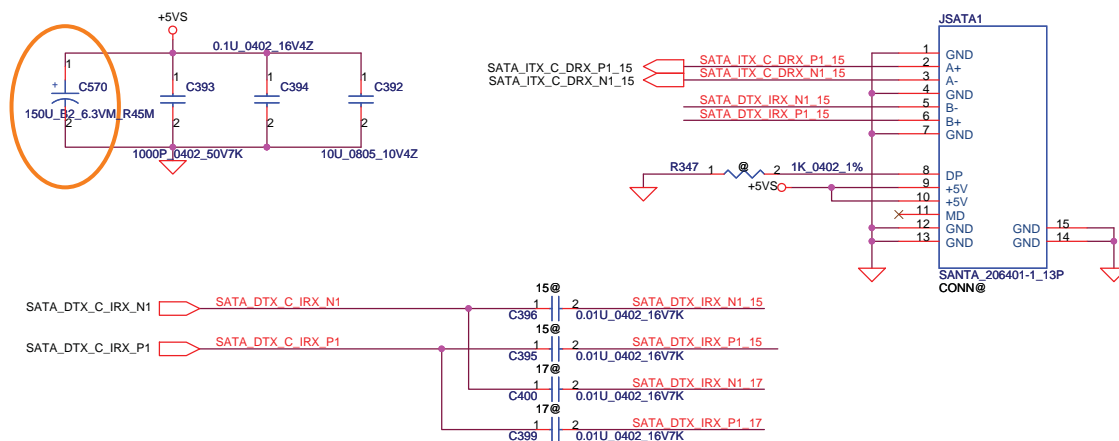




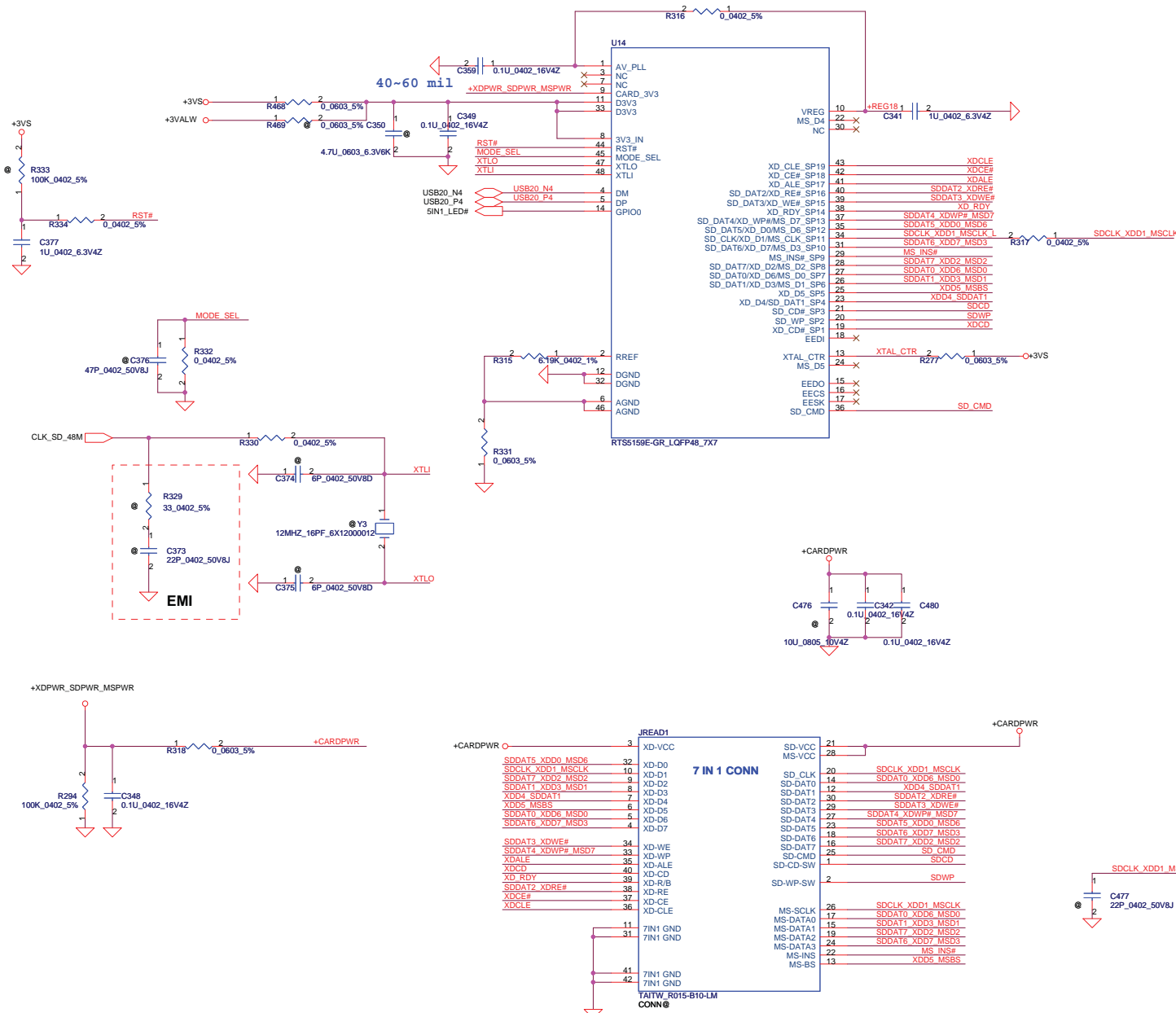
## SATA HDD Conn.



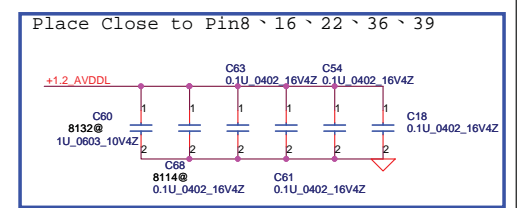
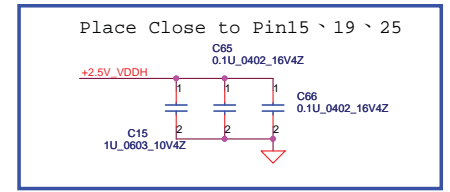
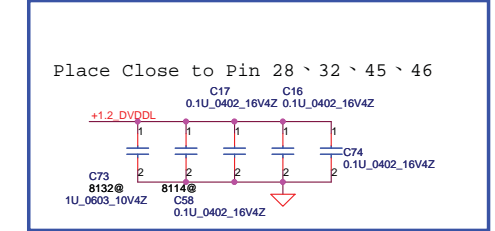
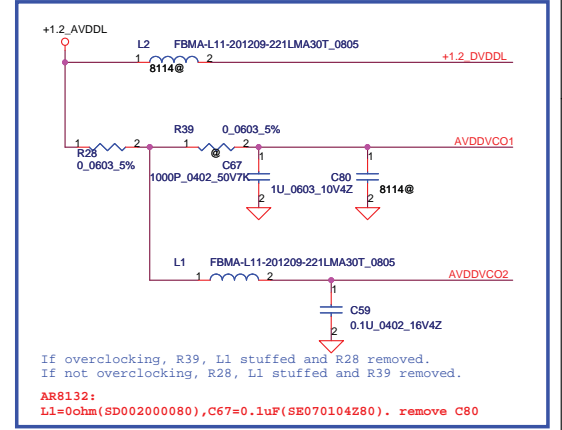
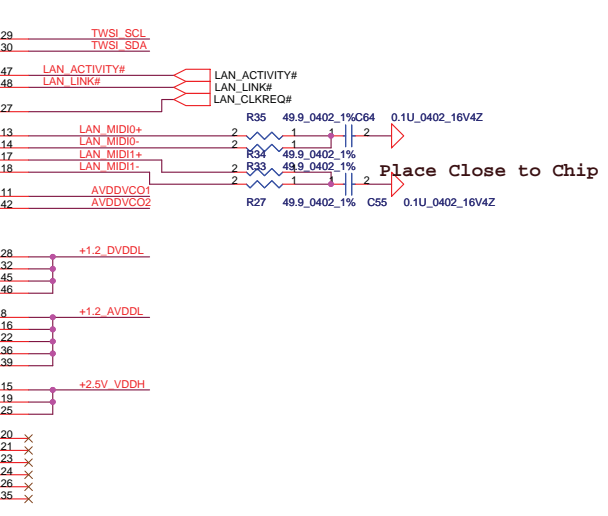
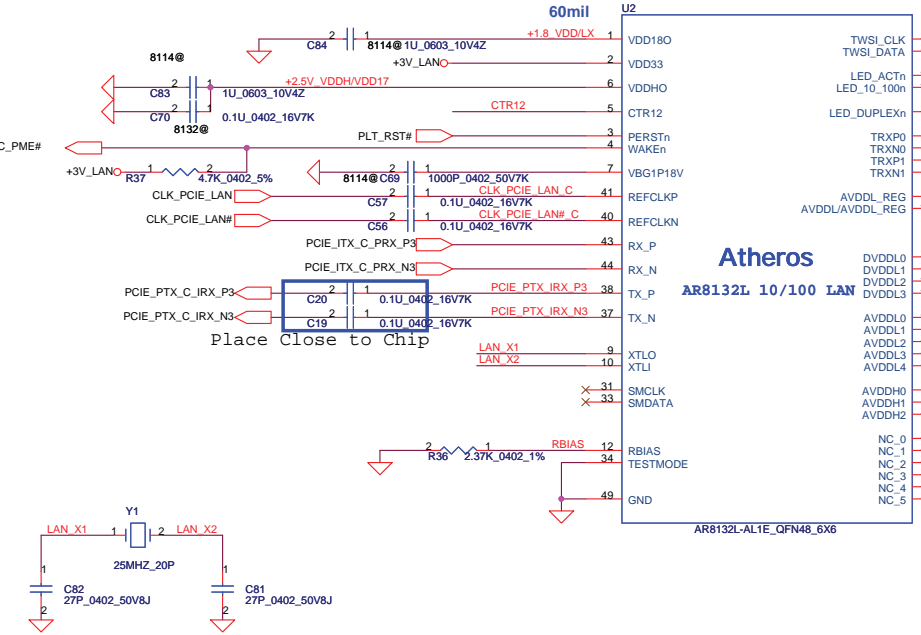
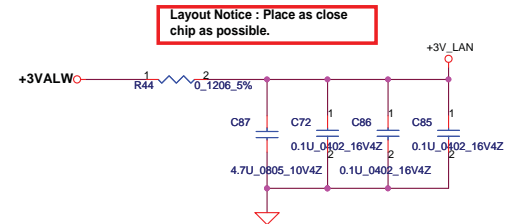
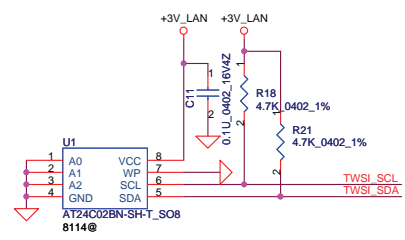
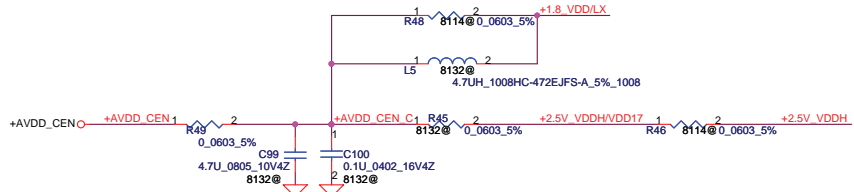
## SATA ODD Conn.

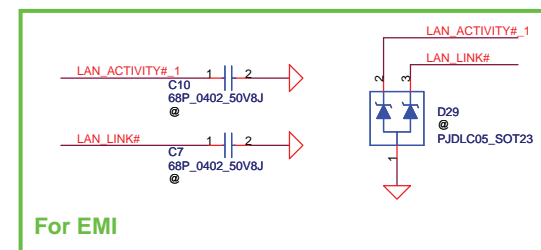
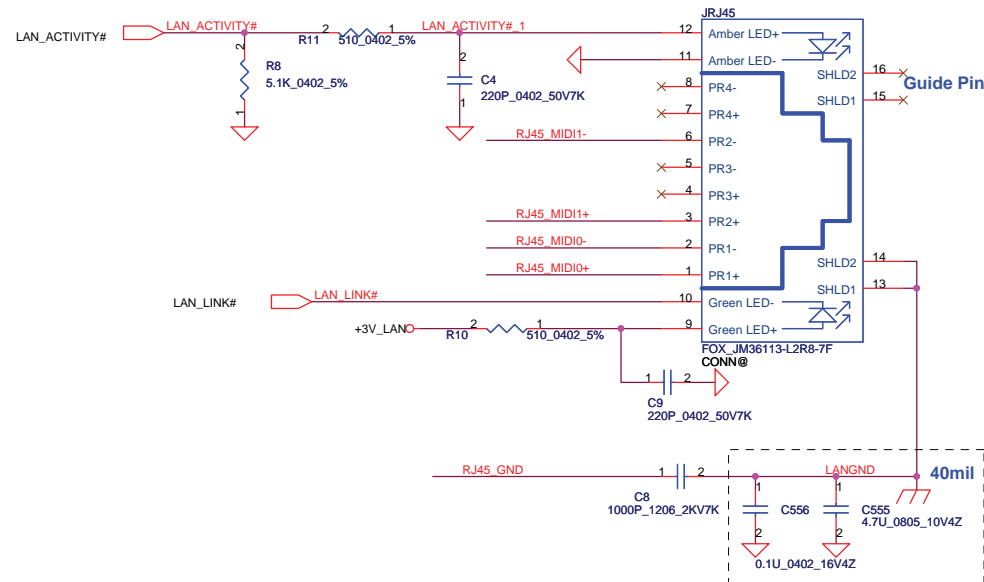
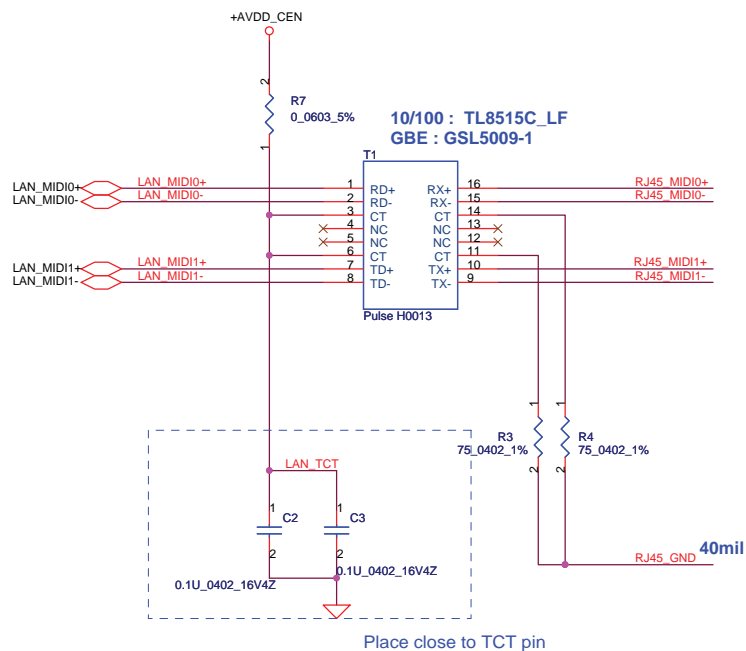


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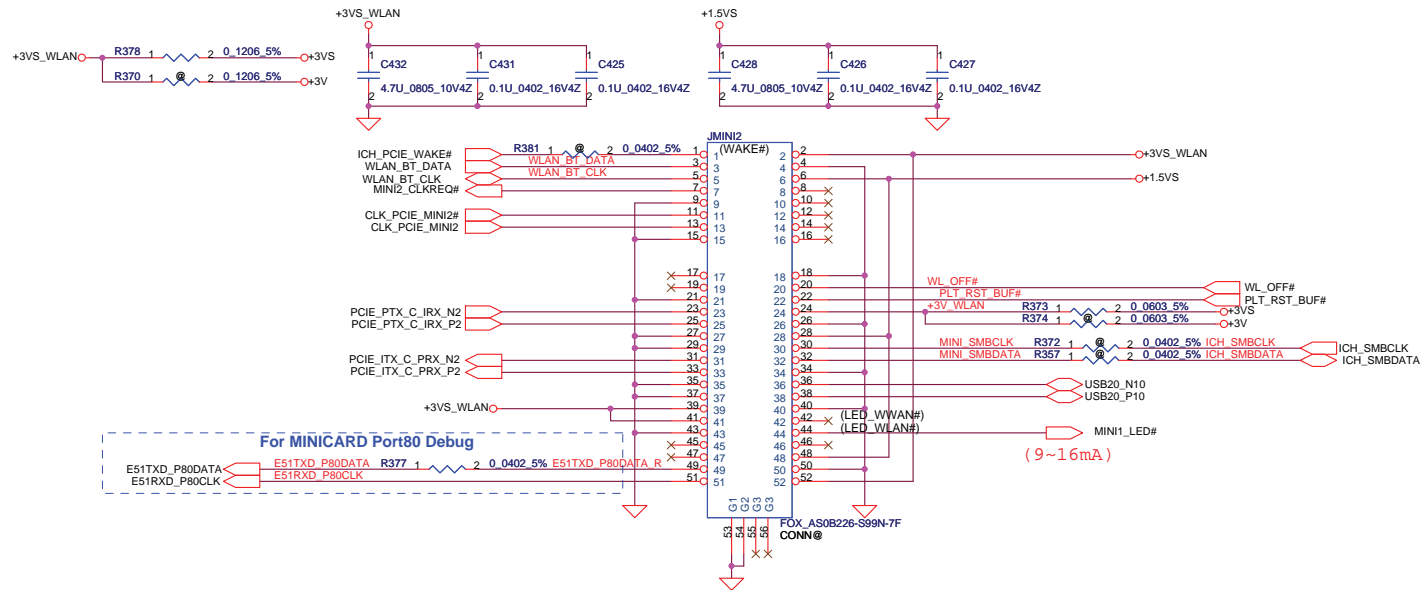
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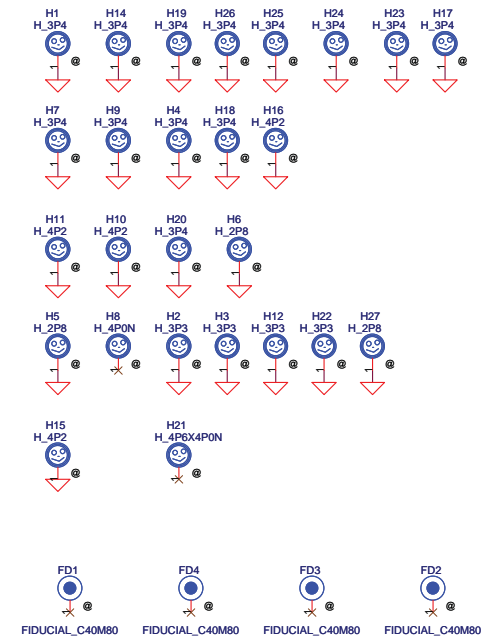


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# For Wireless LAN

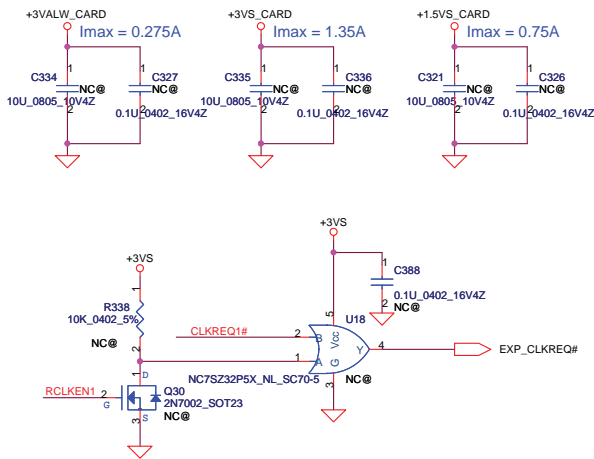
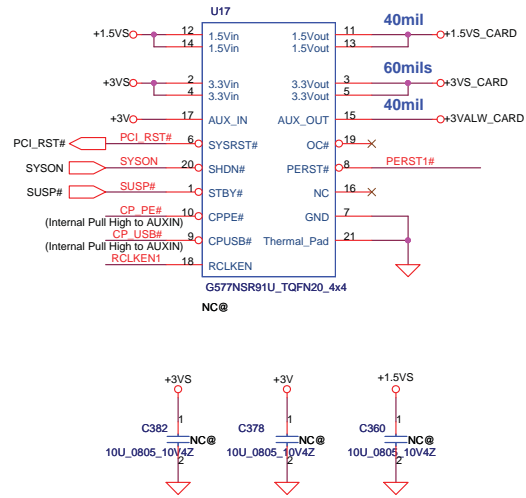


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

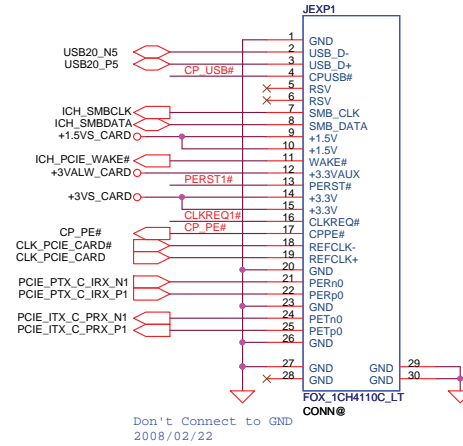


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								Rev B		Document Number		Rev D			
								Date		401636					
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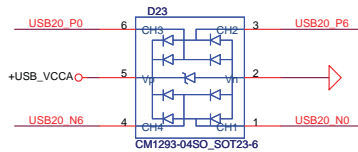
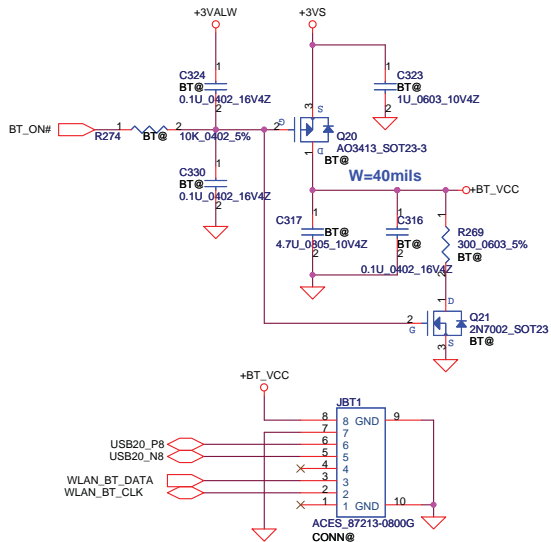
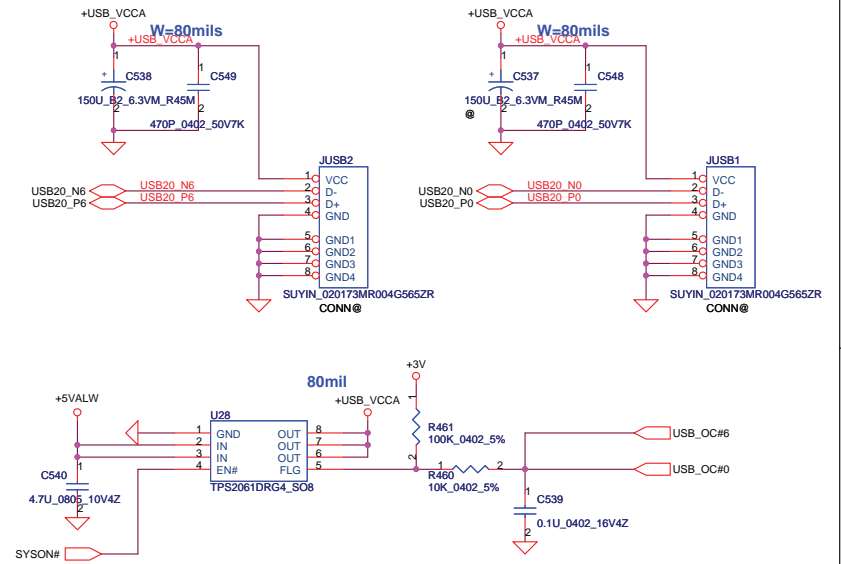
## New Card Power Switch



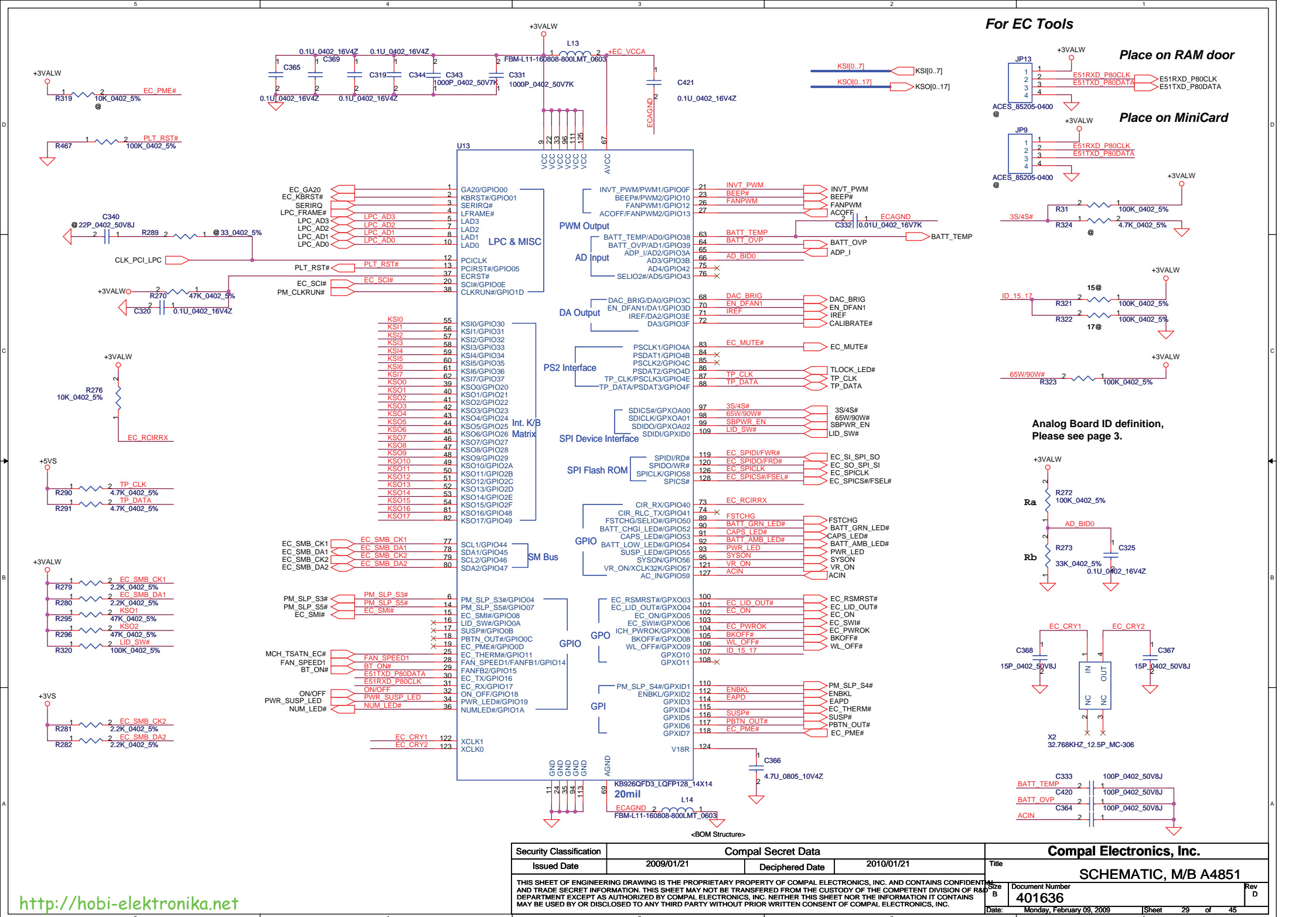
### ***New Card Socket (Left/TOP)***



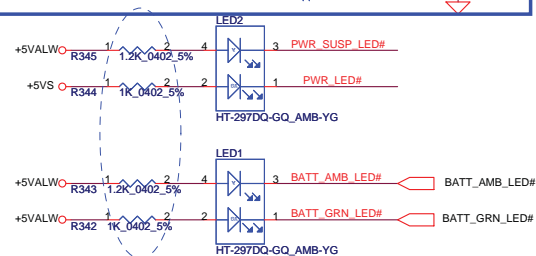
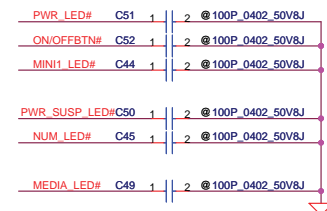
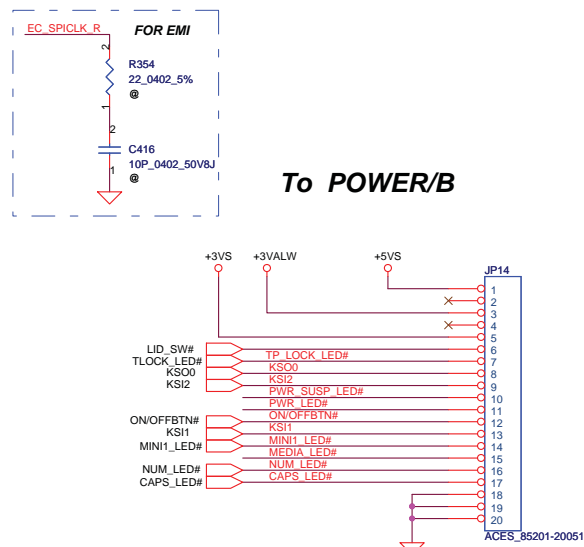
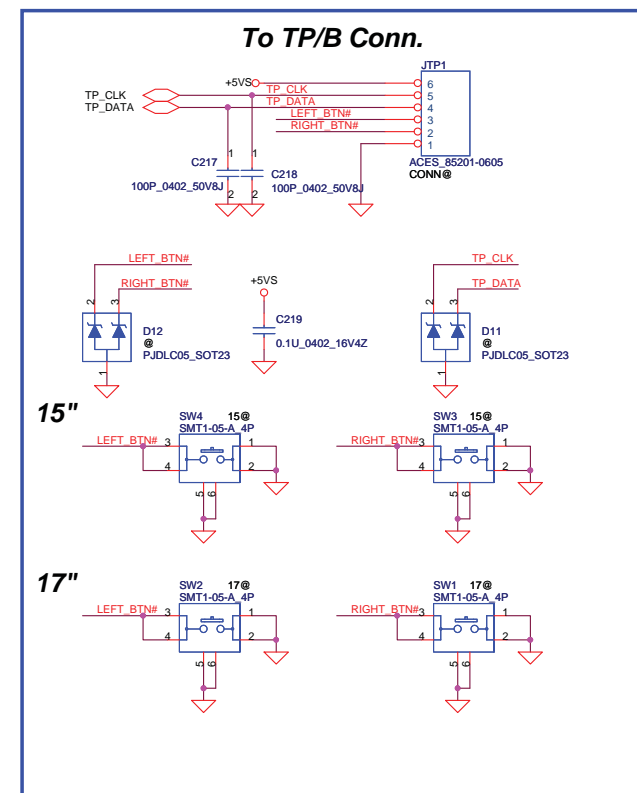
**Bluetooth Conn.**

**USB CONN.**

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								SCHEMATIC, M/B A4851									
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										Doc No		Rev D					
										Document Number							
Date		401636															
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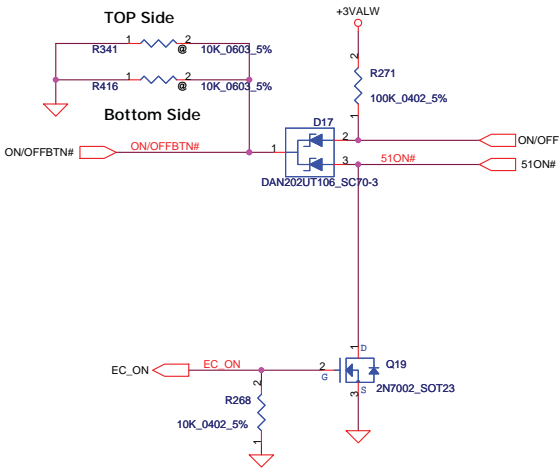
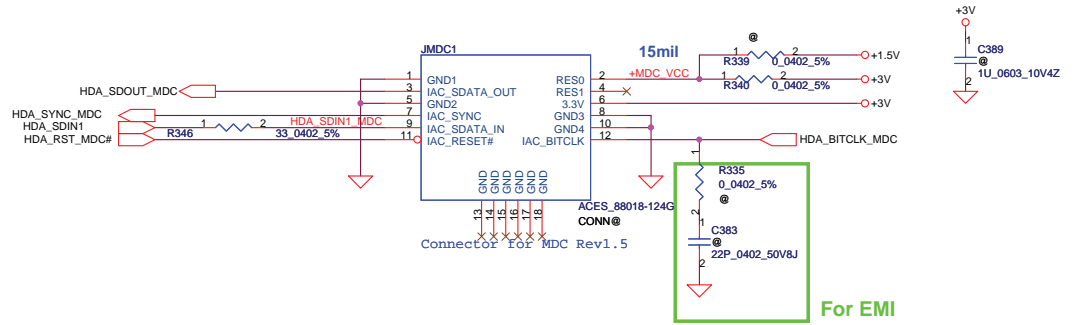




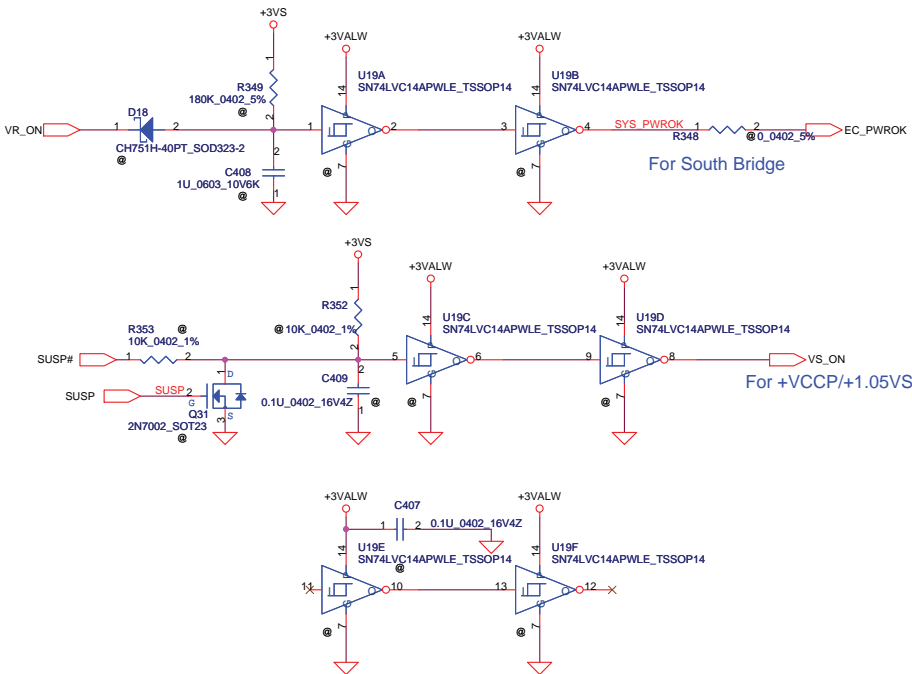
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## Power Button

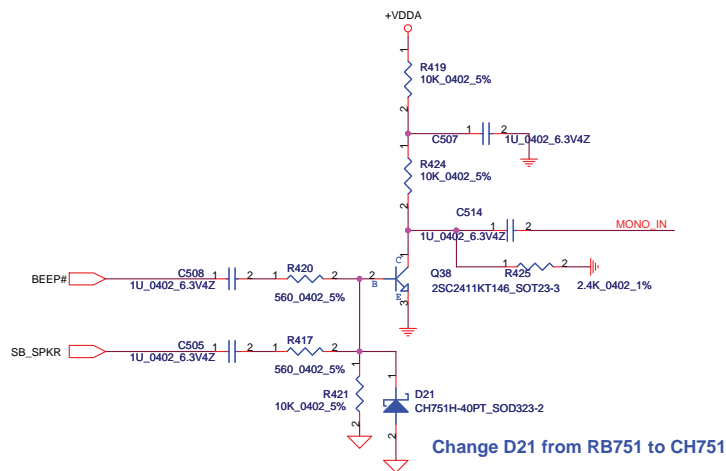
ON/OFF switch

***HDA MDC Conn.***

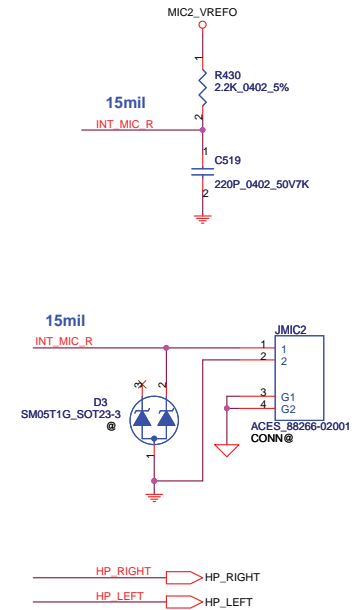
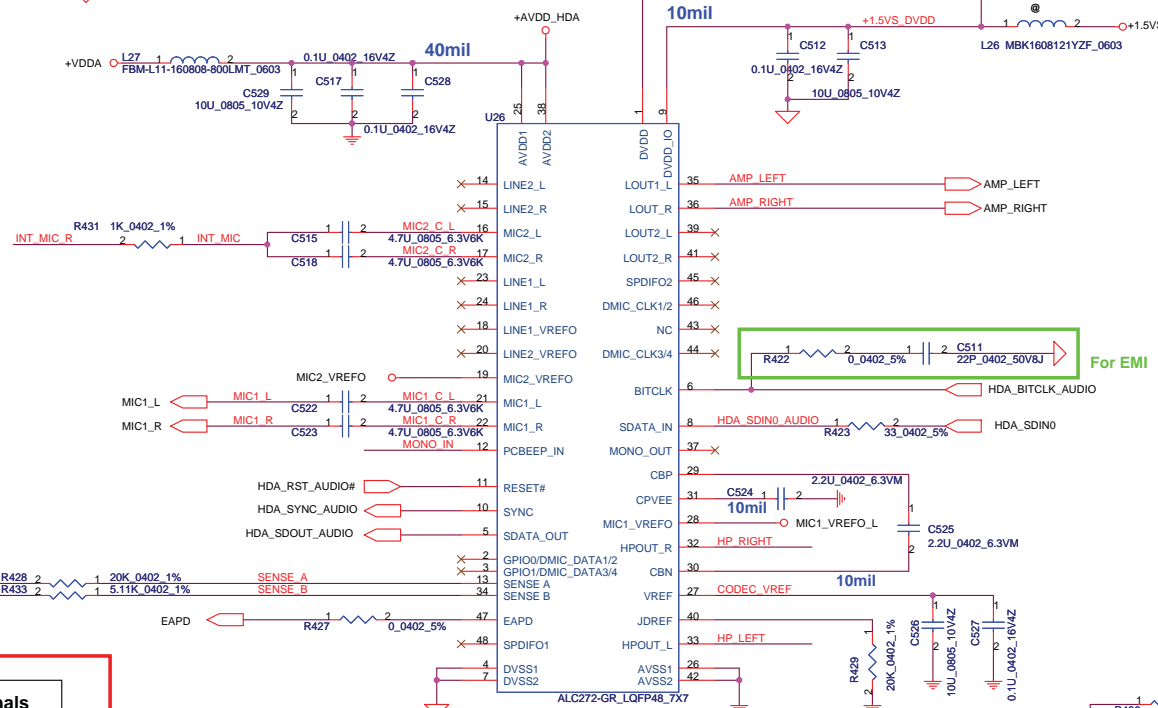
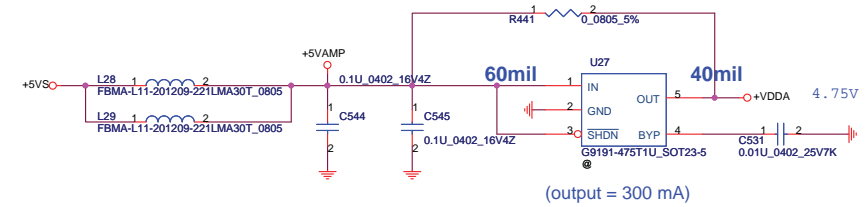
## Power ON Circuit



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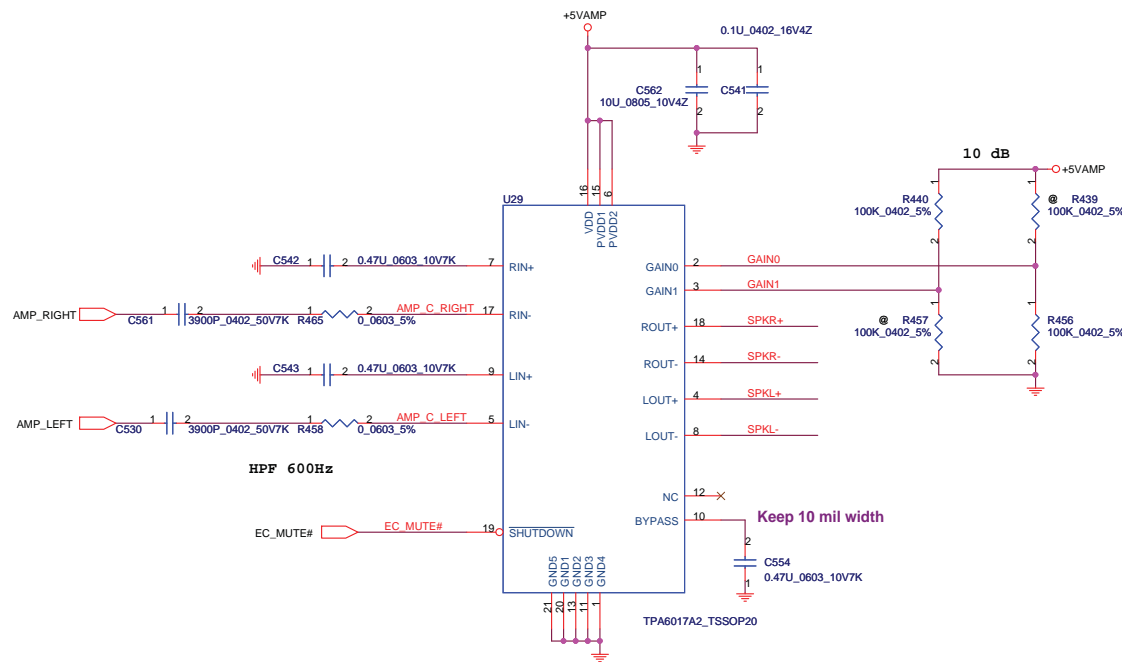


## HD Audio Codec

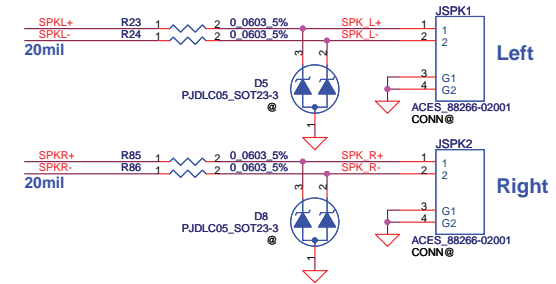


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-B (PIN 21, 22)
	20K	
	10K	
	5.1K	
SENSE B	39.2K	PORT-H (PIN 32,33)
	20K	
	10K	
	5.1K	

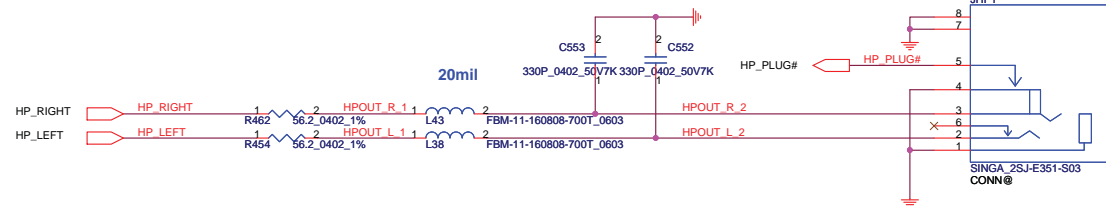
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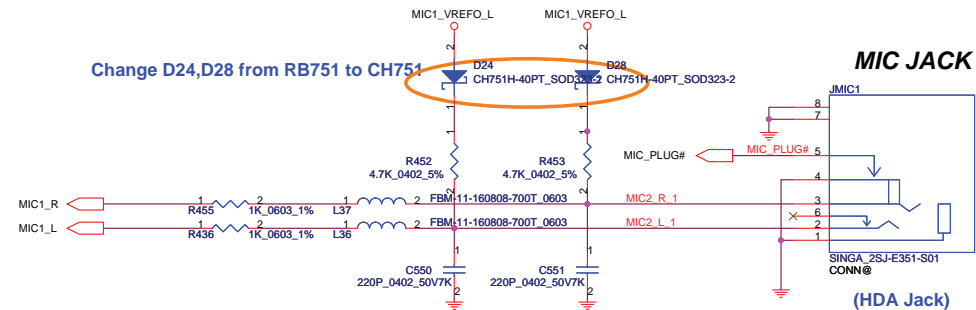
## Int. Speaker Conn.



## LINE Out/Headphone Out

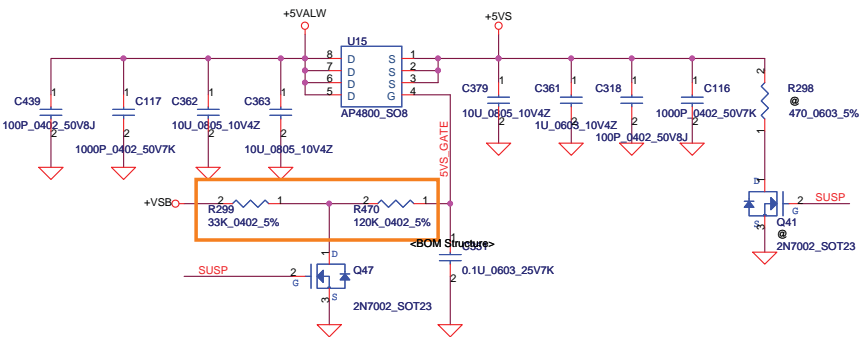


Change D24,D28 from RB751 to CH751

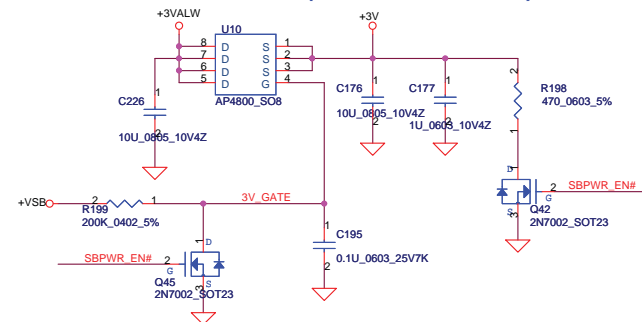


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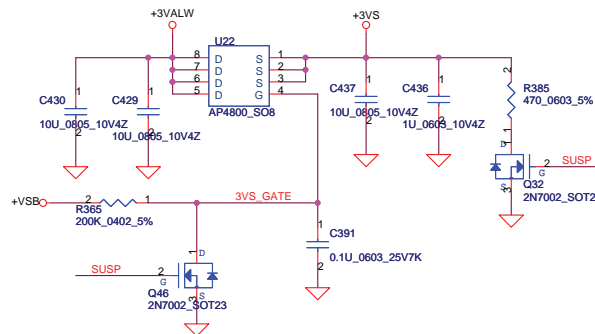
### +5VALW TO +5VS



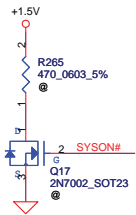
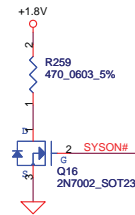
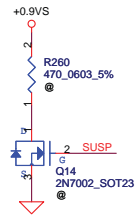
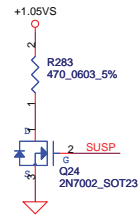
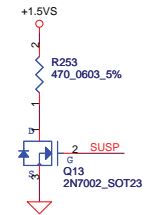
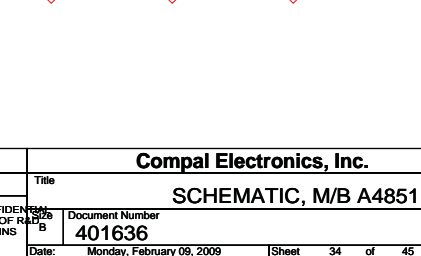
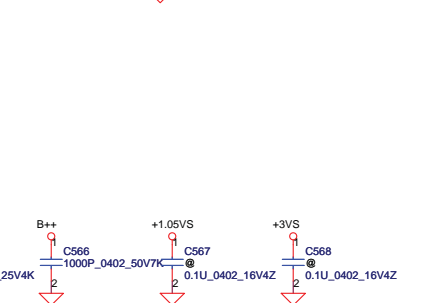
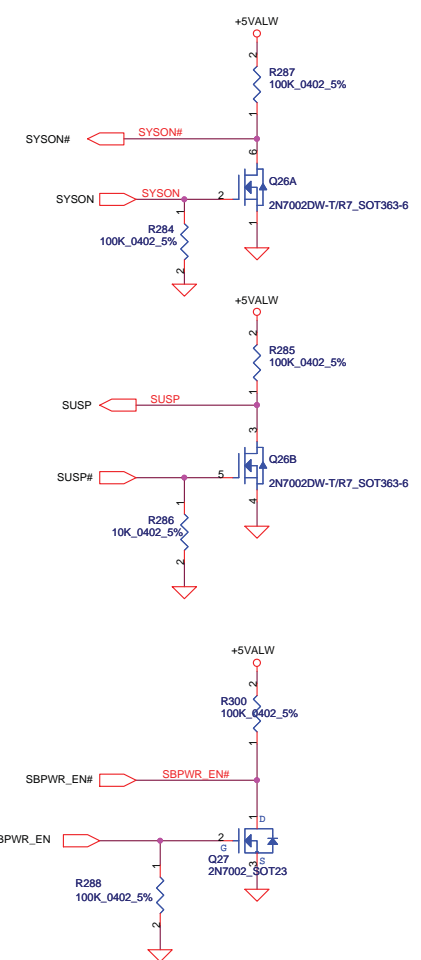
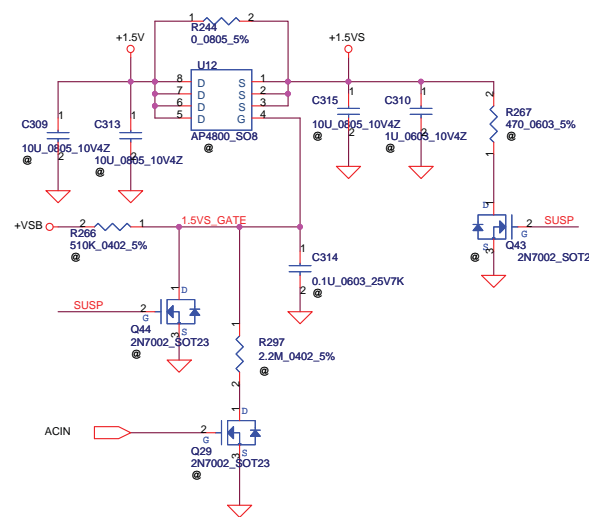
### +3VALW TO +3V\_SB(ICH8M AUX Power)



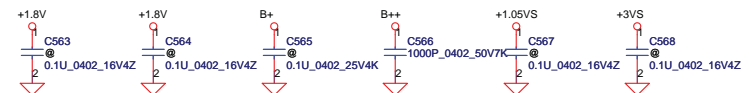
### +3VALW TO +3VS



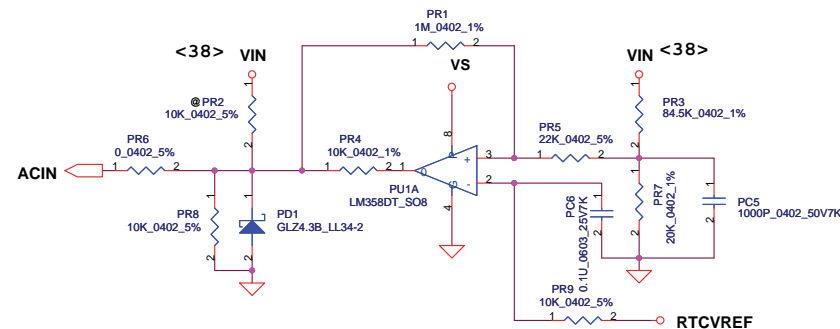
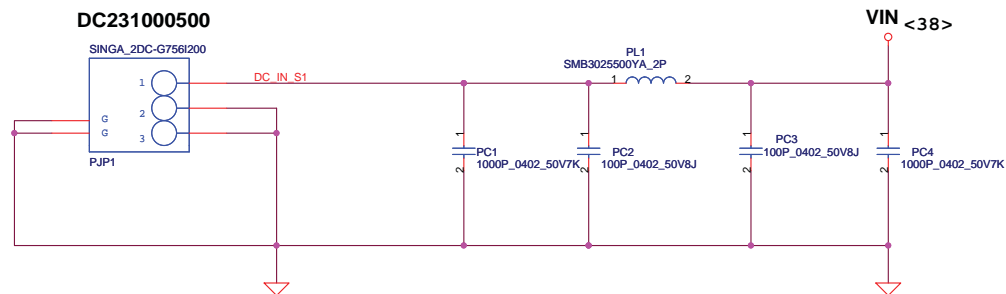
### +1.5V to +1.5VS



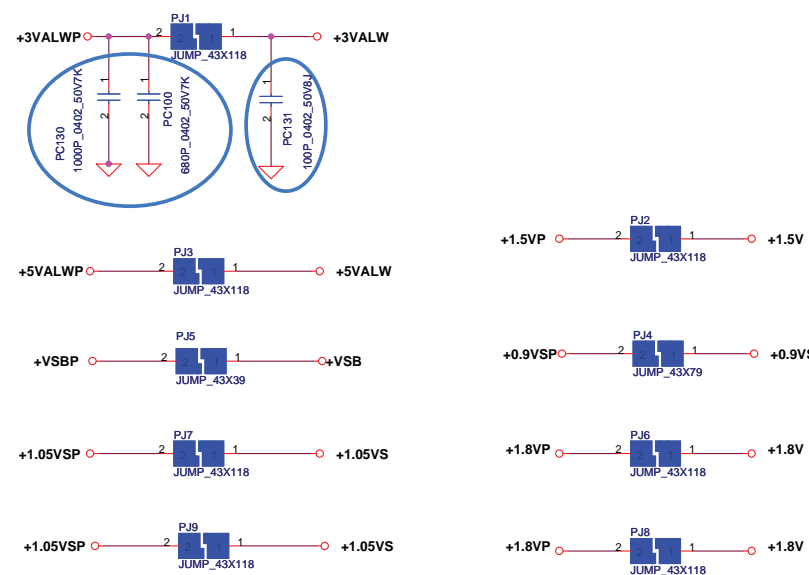
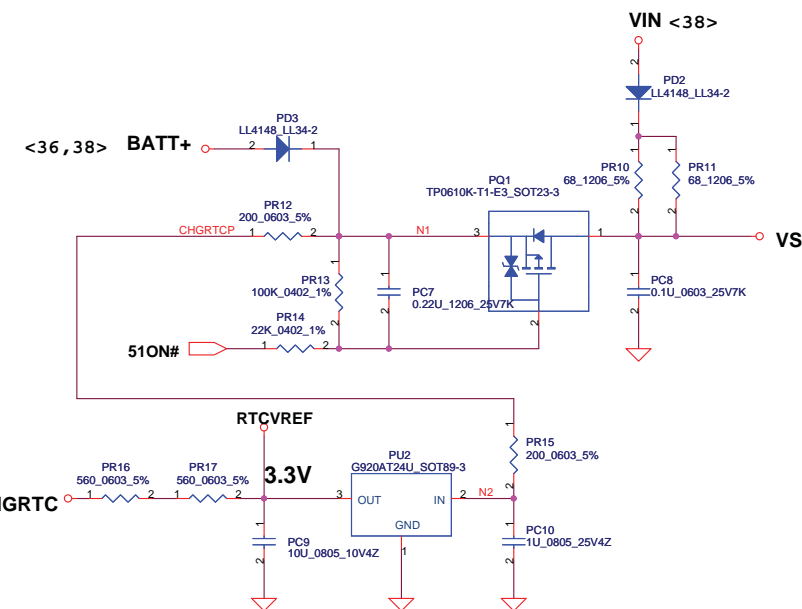
### Reserve for EMI request



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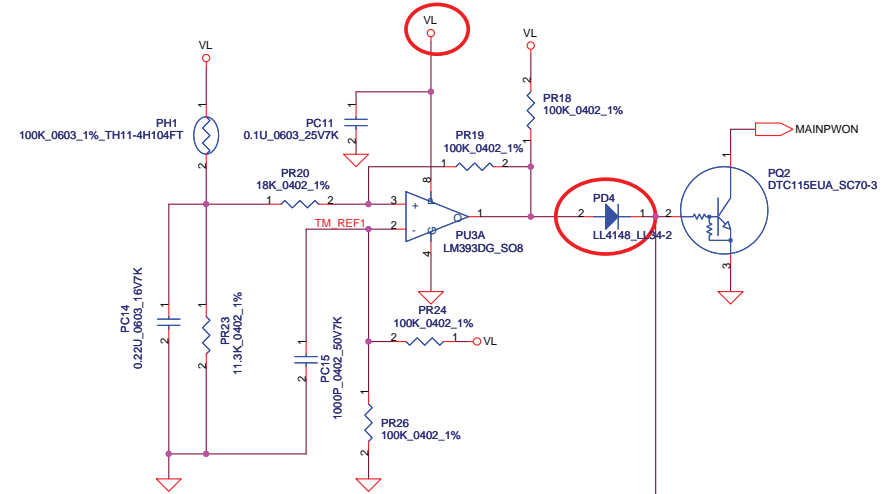
Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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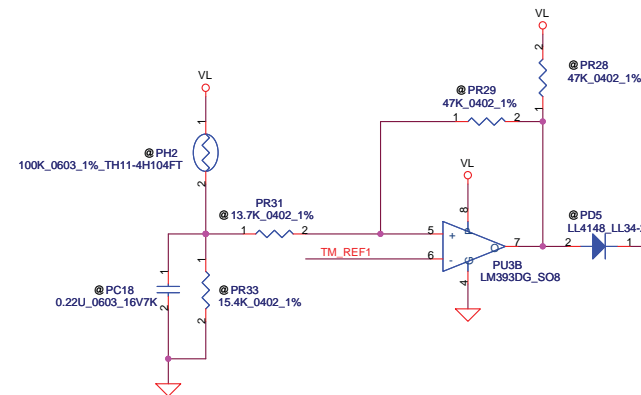
# PH1 under CPU botten side :

CPU thermal protection at 90 degree C  
Recovery at 70 degree C



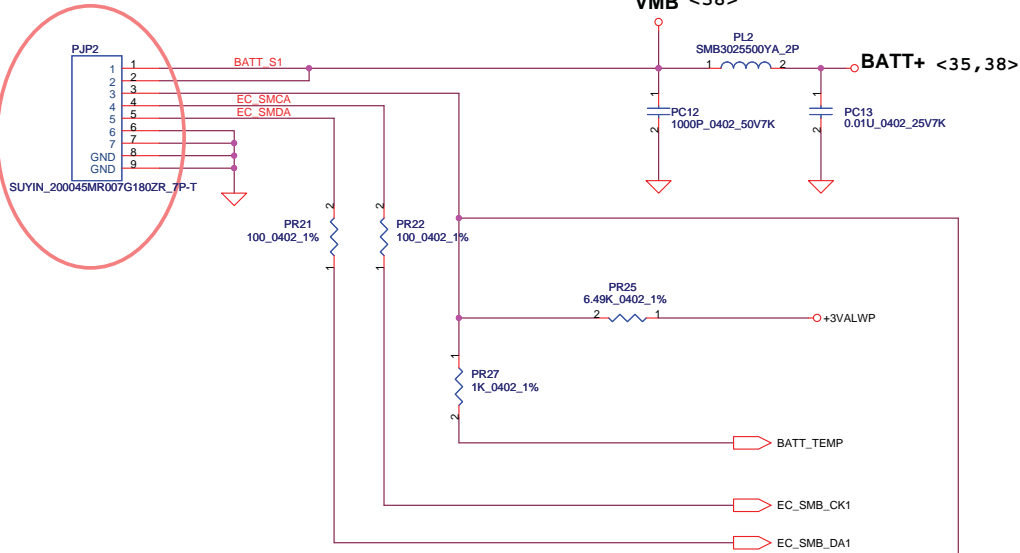
# PH2 near main Battery CONN :

BAT. thermal protection at 90 degree C  
Recovery at 70 degree C

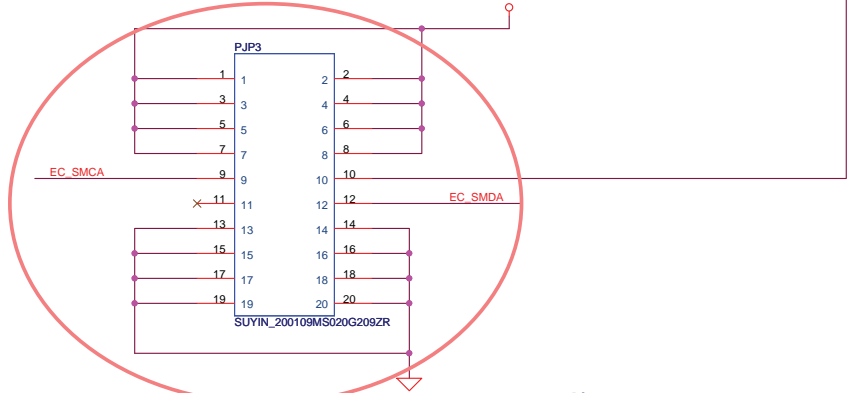


# VMB <38>

# BATT+ <35,38>

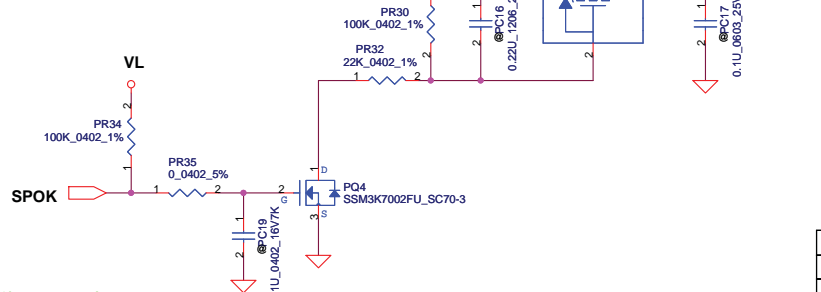


# VMB <38>



# PQ3 TP0610K-T1-E3\_SOT23-3

# B+ <36,37,38,39,40,42>



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**+3VALWP**

**+5VALWP**

**ISL6237\_B+**

**12/25\_DVT\_EMI**

**VS**

**V5VILT**

**V5DRV**

**V5BST**

**V5LL**

**V5DRV**

**V5PGND**

**V5VOUT**

**V5FB**

**V5SKIPSEL**

**V5PGOOD**

**V5TRIP**

**V5GND**

**V5EN\_LDO**

**V5EN1**

**V5EN2**

**V5VREF3**

**V5TONISE**

**V5PC38**

**V5PC39**

**V5PC40**

**V5PQ9**

**V5TP0610K-T1-E3\_SOT23-3**

**V5MAINPWON**

**V5GLZ5.1B\_LL34-2**

**V5PD6**

**V51SS355\_SOD323-2**

**V5PR48**

**V5PC37**

**V5PR53**

**V5PR55**

**V5PR56**

**V5PC38**

**V5PC39**

**V5PC40**

**V5PQ9**

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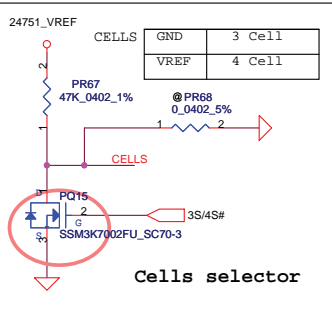
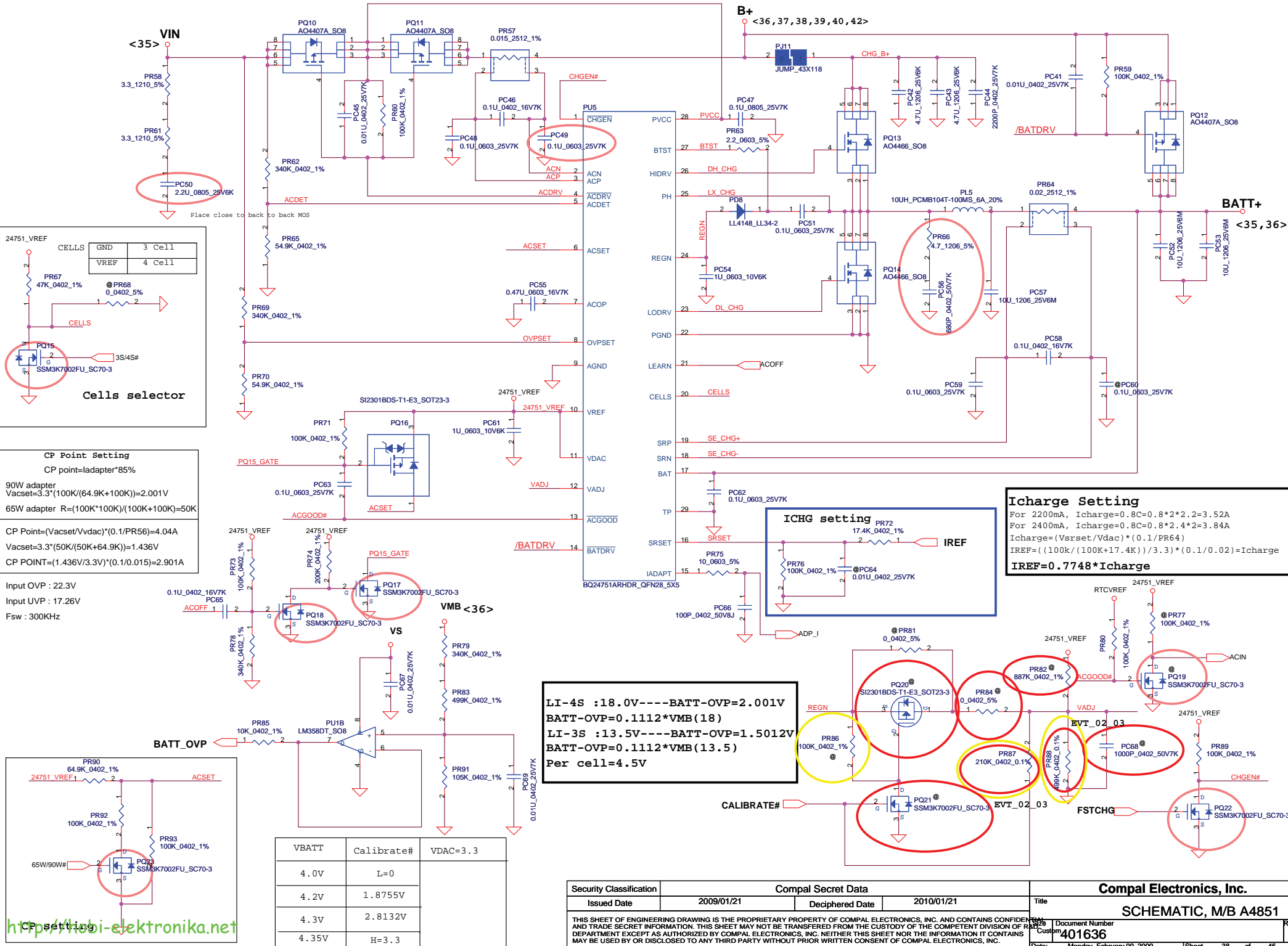
**V5PC40**

**V5PQ9**

**V5TP0610K-T1-E3\_SOT23-3**

**V5MAINPWON**</

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**CP Point Setting**  
CP point=ladder\*85%

90W adapter  
Vacset=3.3\*(100K/(64.9K+100K))=2.001V

65W adapter R=(100K\*100K)/(100K+100K)=50K

CP Point=(Vacset/Vdadc)\*(0.1/PR56)=4.04A

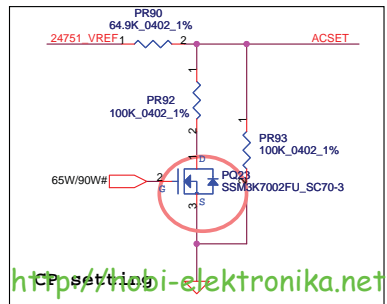
Vacset=3.3\*(50K/(50K+64.9K))=1.436V

CP POINT=(1.436V/3.3V)\*(0.1/0.015)=2.901A

Input OVP : 22.3V

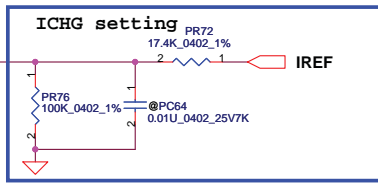
Input UVP : 17.26V

Fsw : 300KHz



VBATT	Calibrate#	VDAC=3.3
4.0V	L=0	
4.2V	1.8755V	
4.3V	2.8132V	
4.35V	H=3.3	

**LI-4S : 18.0V---BATT-OVP=2.001V**  
**BATT-OVP=0.1112\*VMB(18)**  
**LI-3S : 13.5V---BATT-OVP=1.5012V**  
**BATT-OVP=0.1112\*VMB(13.5)**  
**Per cell=4.5V**



**Icharge Setting**

For 2200mA, Icharge=0.8C=0.8\*2\*2=3.52A

For 2400mA, Icharge=0.8C=0.8\*2\*2=3.84A

Icharge=(Vsrset/Vdadc)\*(0.1/PR64)

IREF=((100k/(100K+17.4K))/3.3)\*(0.1/0.02)=Icharge

**IREF=0.7748\*Icharge**

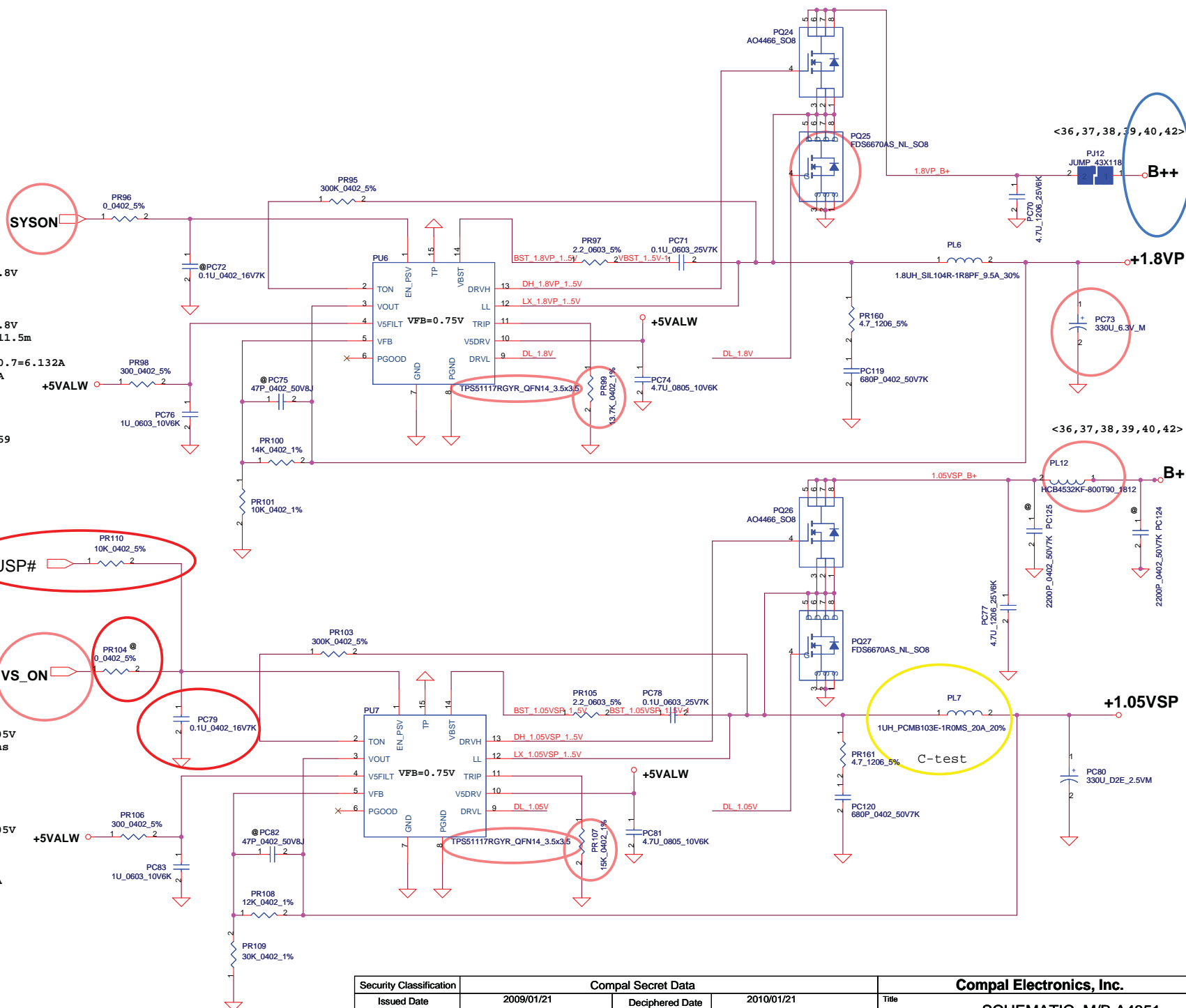
$V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1+PR100/PR101)=0.75 \cdot (1+14K/10K)=1.8V$   
 $F_{sw}=262KHz$  (by Calculation Tool)

$<V_o=1.8V>$   $V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1+PR100/PR101)=0.75 \cdot (1+14K/10K)=1.8V$   
 $F_{sw}=262KHz$   $C_{out} ESR=15m\ ohm$   $R_{dson(max)}=11.5m$   
 $R_{dson(min)}=9m$   
 $I_{peak}=8.76A$  (by power budget),  $I_{max}=I_{peak} \cdot 0.7=6.132A$   
 $\Delta I=\frac{(19-1.8) \cdot (1.8/19)}{(L \cdot F_{sw})}=3.455A$   
 $\Rightarrow 1/2 \Delta I=1.7275A$   
 $V_{trip}=R_{trip} \cdot I_{0uA}=13.7K \cdot 10uA=0.137V$   
 $I_{ocpmin}=V_{trip}/R_{dsonmax}=1.3+1.7275$   
 $=0.137/(0.0115 \cdot 1.3)+1.7275=10.8914A$   
 $I_{ocpmax}=(0.137/(0.009 \cdot 1.1))+1.7275A=15.5659$   
 $I_{ocp}=10.8914-15.5659A$

note: Reference AO4712&TPS51117 spec

$V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1+PR108/PR109)=0.75 \cdot (1+12K/30K)=1.05V$   
 $T_{on}=19 \cdot e^{-12 \cdot 143000 \cdot ((2/3) \cdot V_o + 100mV)/19} + 50ns$   
 $=2.645e-7\ us$   
 $\Rightarrow V_o/V_{in}=D=T_{on}/T_s \Rightarrow T_s=3.35us$   
 $F_{sw}=261KHz$  (by calculation tool)

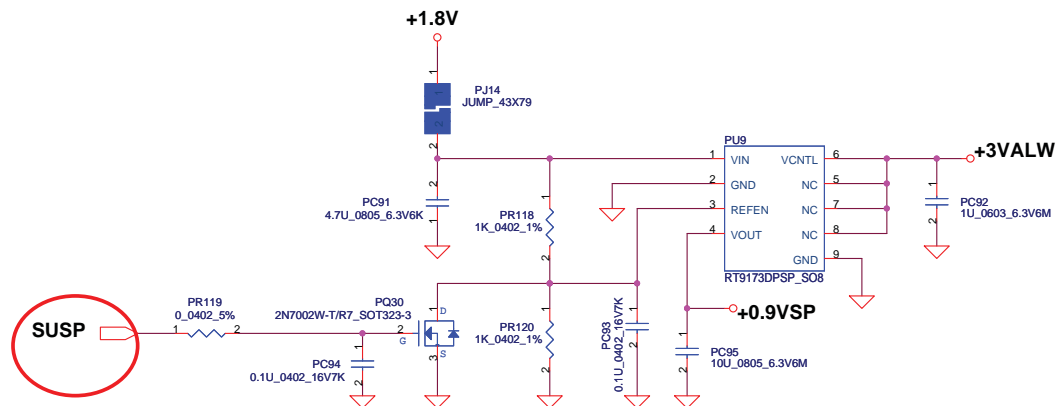
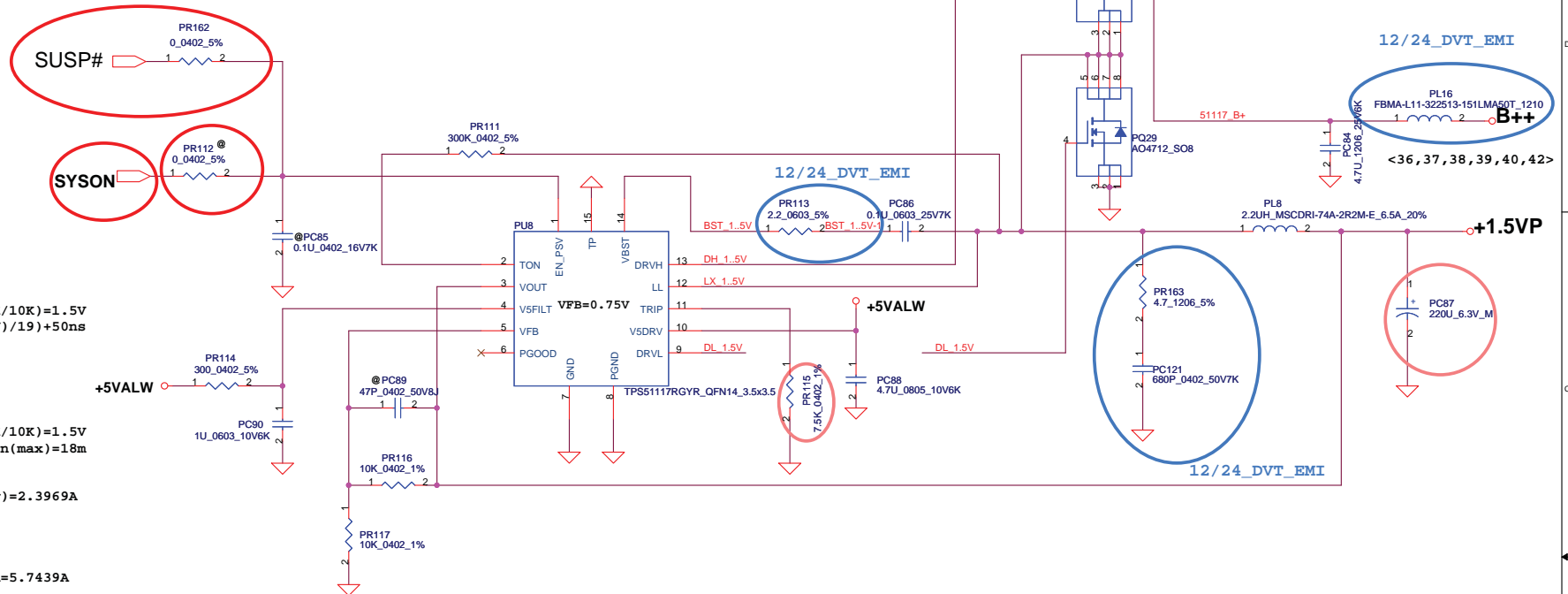
$<V_o=1.05V>$   $V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1+PR108/PR109)=0.75 \cdot (1+12K/30K)=1.05V$   
 $F_{sw}=261KHz$   $C_{out} ESR=15m\ ohm$   
 $R_{dson(max)}=11.5m$   $R_{dson(min)}=9m$   
 $I_{peak}=9A$ ,  $I_{max}=I_{peak} \cdot 0.7=6.3A$   
 $\Delta I=\frac{(19-1.05) \cdot (1.05/19)}{(L \cdot F_{sw})}=2.11A$   
 $\Rightarrow 1/2 \Delta I=1.055A$   
 $V_{trip}=R_{trip} \cdot I_{0uA}=15K \cdot 10uA=0.15V$   
 $I_{ocpmin}=V_{trip}/R_{dsonmax}=1.3+1.055$   
 $=0.15/(0.011 \cdot 1.3)+1.055=11.0892A$   
 $I_{ocpmax}=(0.15/(0.009 \cdot 1.1))+1.055A=16.2073A$   
 $I_{ocp}=11.0892A-16.2073A$



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$V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1+PR116/PR117)=0.75 \cdot (1+10K/10K)=1.5V$   
 $Ton=19 \cdot e^{-12 \cdot 143000 \cdot ((2/3) \cdot V_o + 100mV) / 19} + 50ns$   
 $=2.645e-7 \text{ us}$   
 $\Rightarrow V_o/V_{in}=D=Ton/Ts \Rightarrow Ts=3.35us$   
 $Fsw=262KHz$

$<V_o=1.5V> \quad V_{FB}=0.75V$   
 $V_o=V_{FB} \cdot (1+PR116/PR117)=0.75 \cdot (1+10K/10K)=1.5V$   
 $Fsw=262KHz \quad C_{out} ESR=15m \text{ ohm} \quad R_{dson}(max)=18m$   
 $R_{dson}(min)=15m$   
 $I_{peak}=3.51A, \quad I_{max}=2.457A$   
 $\Delta I = ((19-1.5) \cdot (1.5/19)) / (L \cdot Fsw) = 2.3969A$   
 $\Rightarrow 1/2 \Delta I = 1.198A$   
 $V_{trip}=R_{trip} \cdot I_{0uA}=7.5K \cdot 10uA=0.075V$   
 $I_{ocpmin}=V_{trip}/R_{dsonmax} \cdot 1.2+1.198$   
 $=0.075 / (0.018 \cdot 1.3) + 1.198 = 4.4035A$   
 $I_{ocpmax}=(0.075 / (0.015 \cdot 1.1)) + 1.198A = 5.7439A$   
 $I_{ocp}=4.4035A \sim 5.7439A$



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Add PC57 :10U_1206_25V_6M	0.1	38	Add PC57 :10U_1206_25V_6M	20080902	EVT
2		Add snubber for EMI	0.1	42	Add snubber for EMI	20080915	EVT
3		Shift PC99 from +cpu_B+ to B+	0.1	42	Shift PC99 from +cpu_B+ to B+	20080915	EVT
4		Add PJ15 to B+	0.1	39	Add PJ15 to B+	20080915	EVT
5		PR135 and PR140 change to 0_0603_5%	0.1	42	PR135 and PR140 change to 0_0603_5%	20080915	EVT
6	Charger feedback trace too long	ADD PC49	0.2	38	ADD PC49	20081124	DVT
7	Power sequence error	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	0.2	40	+1.5VP: enable pin change from SUSP# to SYSON +0.9VSP: enable pin change from SUSP# to SUSP	20081124	DVT
8	Load line over spec	PR131: change to 5.76K_0402_1%	0.2	42	PR131: change to 5.76K_0402_1%	20081124	DVT
9	3D hang	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	0.2	38	Charger PR63:change to 2.2_0603_5% PR66:Add 4.7_1206_5% PC56:Add 680P_0402_50V7K	20081124	DVT
10	3D hang	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	0.2	39	+1.8VP PR97:change to 2.2_0603_5% PR160:Add 4.7_1206_5% PC119:Add 680P_0402_50V7K	20081124	DVT
11	3D hang	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	0.2	39	+1.05VSP PR105:change to 2.2_0603_5% PR161:Add 4.7_1206_5% PC120:Add 680P_0402_50V7K Add bead between B+ and 1.05VSP_B+	20081124	DVT
12	EMI solution	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	0.2	37	+5VALW/+3VALW PR37: Add 4.7_1206_5% PR41: Add 4.7_1206_5% PC33: Add 680P_0402_50V7K PC34: Add 680P_0402_50V7K PR38: change to 2.2_0603_5% PR39: change to 2.2_0603_5%	20081124	DVT
13	EMI solution	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	0.2	42	+CPU CORE PR158: Add 4.7_1206_5% PR159: Add 4.7_1206_5% PC117: Add 680P_0402_50V7K PC118: Add 680P_0402_50V7K PR135: change to 2.2_0603_5% PR140: change to 2.2_0603_5%	20081124	DVT
16	EMI solution	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	0.2	42	+CPU CORE PC122: Reserve 2200P_0402_50V7K on B+	20081124	DVT
17	EMI solution	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	0.2	39	+1.05VSP PR105 : change to 2.2_0603_5% PL12 : Add HCB4532KF-800T90_1812 PC124: Reserve 2200P_0402_50V7K on B+ PC125: Reserve 2200P_0402_50V7K on B+	20081124	DVT

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
18	Battery & HW solution	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%  +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K  +1.5VP PR112: Reserve(@) 0_0402_5%	0.2	38 39 40	Charger PQ20:Reserve(@)SI2301BDS-T1-E3_SOT23-3 PQ21:Reserve(@)SSM3K7002FU_SC70-3 PR82:Reserve(@)887K_0402_1% PR84:Reserve(@)0_0402_5% PC68:Reserve(@)1000P_0402_50V7K PR87:change to 210K_0402_1% PR88:change to 499K_0402_1%  +1.05VSP PR104: Reserve(@)0_0402_5% PR110: change to 10K_0402_5% PR79 : Add 0.1U_0402_16V7K  +1.5VP PR112: Reserve(@) 0_0402_5%	20081124	DVT
19	EMI soultion	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	0.3	35 40	+3VALWP/+3VALW PC100: 680P_0402_50V7K PC130: 1000P_0402_50V_7K PC131: 1000P_0402_50V_8J +1.5VP ADD PR113: 2.2_0603_5% ADD PR163: 4.7_1206_5% ADD PC121: 680P_0402_50V7K ADD PL16 :FBMA-L11-322513-151LMA50T_1210	20081224	PVT
20	POWER Solution	+3VALWP/+5VALWP  RT8206- Fix output 5V for HW no HDMI	0.3	37	+3VALWP/+5VALWP PR42: Reserve 61.9K_0402_1%	20090111	PVT

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Item	Fixed Issue	Reason for change	Rev	PG#	Modify List	Date	Phase
21	EMI solution	Reduce the Noise	0.3	37	Add PL 13 ( HCB4532KF-800T90_1812) Add PL 14 ( FBMA-L11-322513-151LMA50T_1210) Add PL 15 ( FBMA-L11-322513-151LMA50T_1210) Add PC126 ( 100P_0402_50V8J) Add PC128 ( 100P_0402_50V8J) Add PC129 ( 1000P_0402_50V7K)	20090112	PVT
22	Battery solution	Adjust battery voltage	0.3	38	Reserve PR86 ( 100K_0402_1%)	20090112	PVT
23	Saturation current	1.8u choke saturation current too small	0.3	39	change PL7 to 1UH_PCMB103E-1R0MS_20A_20%	20090113	PVT
24	GP BOM	Tolerance: K:+-10% ; J:+-5%	0.4	42	Change PC106 to 33P_0402_50V8J Change PC108 to 33P_0402_50V8J Change PC110 to 33P_0402_50V8J Change PC114 to 33P_0402_50V8J	20090123	PVT
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- 11/11
- 1. Page 17;Un-POP R412,Q35
  - 2. Page 32;Un-POP R340,POP R339
  - 3. Page 32;Un-POP D3
  - 4. Change C13,C269,C282,C482 P/N to SGA1933D10 (ESR From 15 to 9 ohm)
  - 5. DEL HDMI Schematic (del HDMI@/NHDMI@)

- 11/19
- 1. Change C538,C539 to B size 150U
  - 2. POP D11,D12,D29 and change P/N to SCA00000A00

- 11/24
- 1.Add LAN\_CLKREQ# on CLK Gen and AR8132

- 11/25
- 1.Add C563~C568 for EMI request
  - 2.Add L44 for EMI request
  - 3.Add +3VS and +3V for SB HDA bus
  - 4.Add 0 ohm resistor for Audio DVDD\_IO bus
  - 5.Add 0 ohm between +1.5V and +1.5VS
  - 6.Add 3VS\_GATE schematic on +3VALW to +3VS
  - 7.remove c318 and D16
  - 8.add R400 and C439 for soft-off
  - 9.add R244 to connect +1.5v to +1.5vs

- 11/25
- 1. Change R325,R311 Form 11ohm to 22 ohm
  - 2. Change D21,D24,D28 from RB751 to CH751
  - 3. Reserve C485,C282

- 12/18
- 1. Change R299 to 47K,ADD R470 (100K)

- 1/20
- 1. Change R299 to 22K and R470 to 120K
  - 2. Add R570 (150U) in pgae 23
  - 3.change board ID R273 to 33K

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